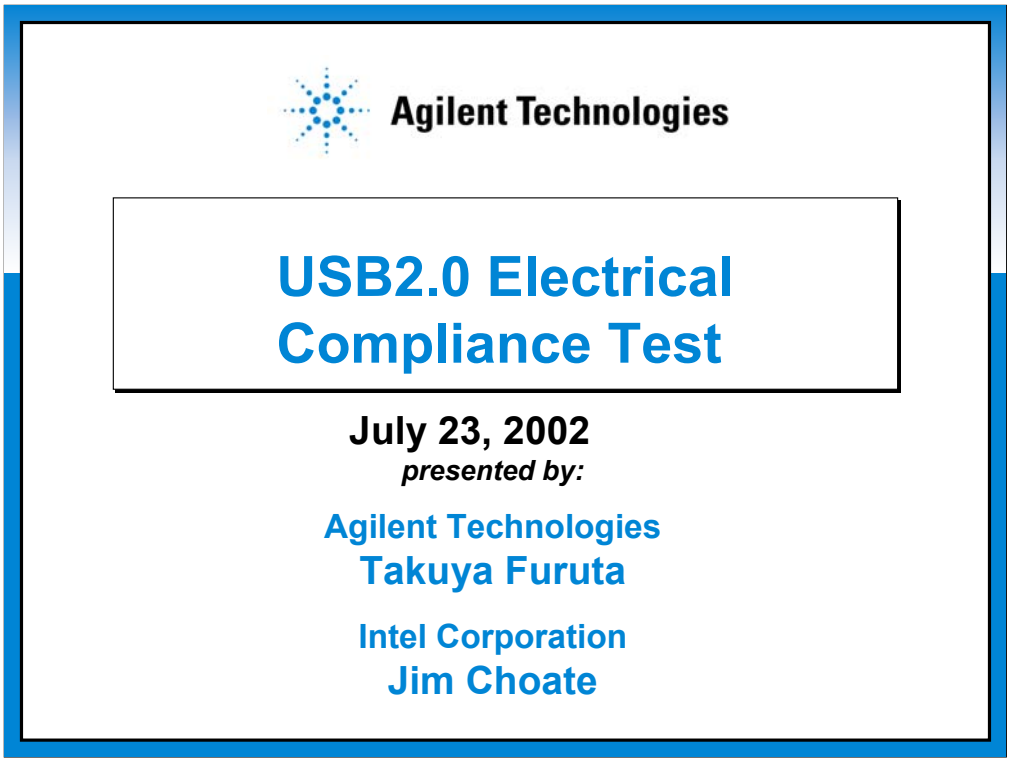
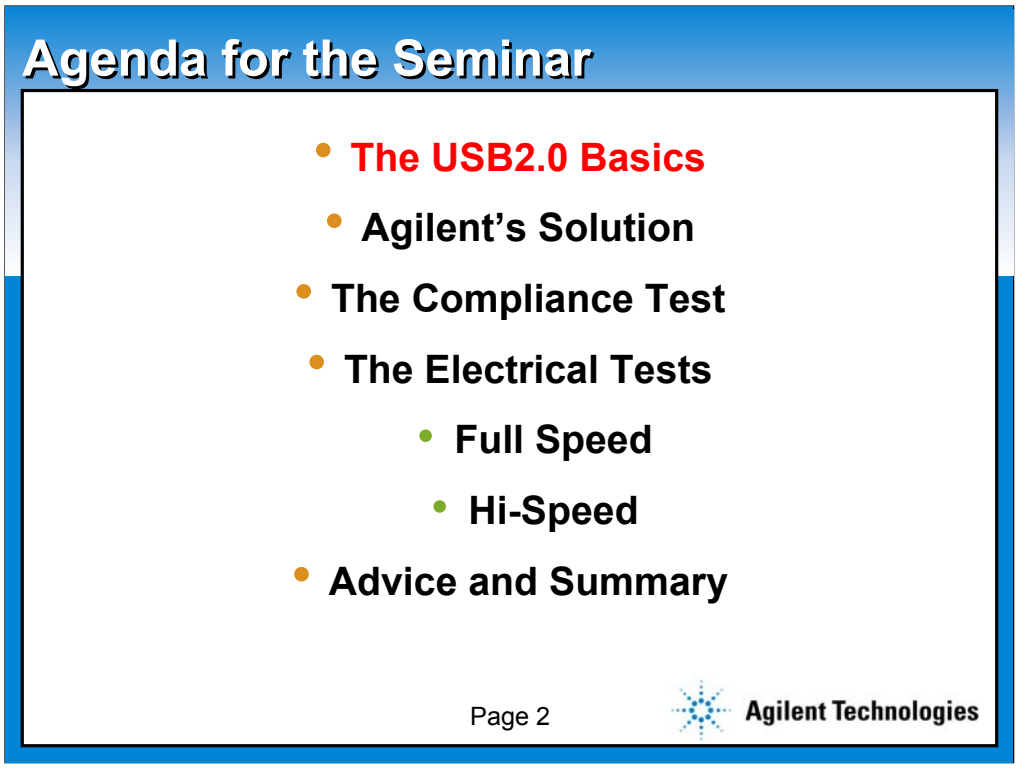


Hi, my name is Takuya Furuta, a Market Development Manager for Agilent Technologies. First of all, thank you all for attending the e-Seminar "USB2.0 Electrical Compliance Test" by Agilent Technologies. Jim Choate of Intel Corporation will be coordinating the seminar with me, mainly responsible for Q&A section.

As everyone knows, the Universal Serial BUS ver 2.0, which is widely known as USB2.0, is an exciting new technology for the PC environment. Let us start our discussion about the electrical world of USB2.0.

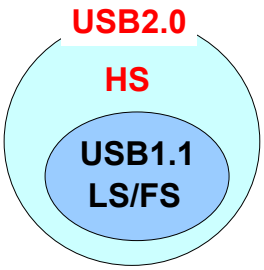


The following will be the agenda for today. We will start with some basics of UB2.0, briefly explain about Agilent solution, discuss the overview of the compliance test, and finally do a deep dive explanation of the electrical tests.

USB2.0 Basics – General

Universal Serial Bus (USB) 2.0:

- All USB specification is owned by USB-IF (Implementaters Forum, Inc.)
- USB2.0 is an EXTENSION of USB1.1
- USB-IF states USB2.0 is the CURRENT ver. of the USB. USB1.1 is available for historical reference only.



USB2.0 Has 3 Transfer Speeds

- Low Speed (LS) = 1.5Mbps
- Full Speed (FS) = 12Mbps
- Hi-Speed (HS) = 480Mbps

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In the beginning, we would like to discuss some basics of USB2.0 to refresh some of your memories. For those who'll be designing the USB for the first time, this will be a good point to start.

First of all it is very important that the USB is a specification owned by a group called USB Implementers Forum, which is known as a USB-IF. For understanding the USB2.0, it is best to think it as an extension of USB1.1. As it said on the slide, USB-IF now states that the current version of USB is USB2.0, and you may only use USB1.1 as a historical reference.

In another words, USB2.0 will have three different speeds, namely Low Speed, running at 1.5Mbps, Full Speed, running at 12Mbps, and finally hi-speed running at 480Mbps. So, since the introduction of USB2.0, all USB designs should follow the USB2.0 specification and should be referred as USB2.0 products, regardless of its speed.

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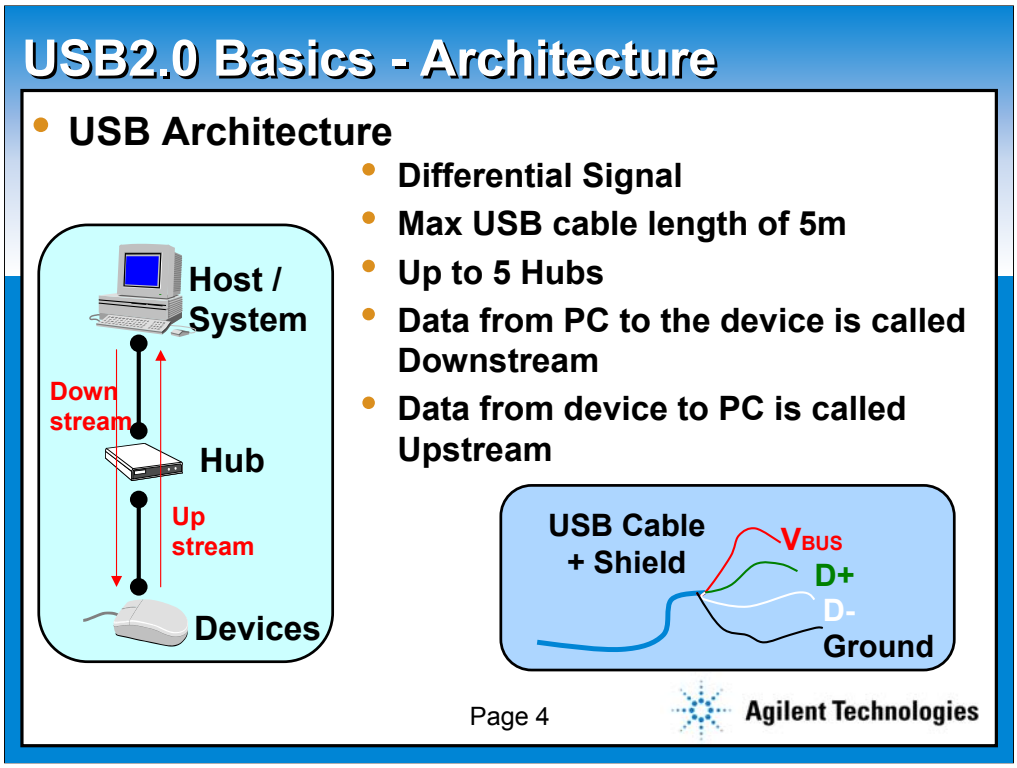


This slide will illustrates the basics on the USB architecture. First of all, USB has a three layered architecture, which consists of Host, Hub and Device. The data sent from a host to a device is called "downstream", and a data sent from the device to a host is called "upstream". It is very important to understand these terminologies, as it would be used often in the USB world.

Some of other important characteristics of USB are:

- it is a differential signal

- one can use up to 5m USB cable

- up to 5 hubs can be used in between

- the cable consists of 4 lines, Vbus, D+, D- and Ground

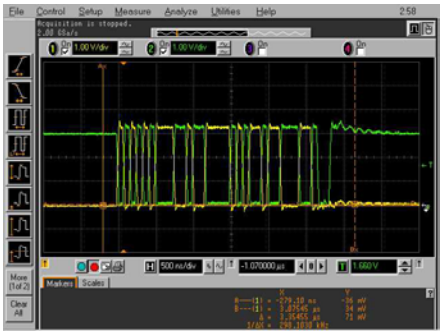
Moving on to page 5.

Vbus = supplies the power

D+, D- = data transfer

Ground = provide the ground

USB2.0 Basics - Signal Rates & Levels



	Low Speed	Full Speed	Hi-Speed
Sig Rate	1.5Mbps	12Mbps	480Mbps
Sig Level	3.3V	3.3V	400mV
Rise Time	75ns < Tr <300ns	4ns < Tr < 20ns	Tr < 500ps
Calculated Min. requirement for Bandwidth (BW = 0.35/Tr)	5MHz	90MHz	1GHz

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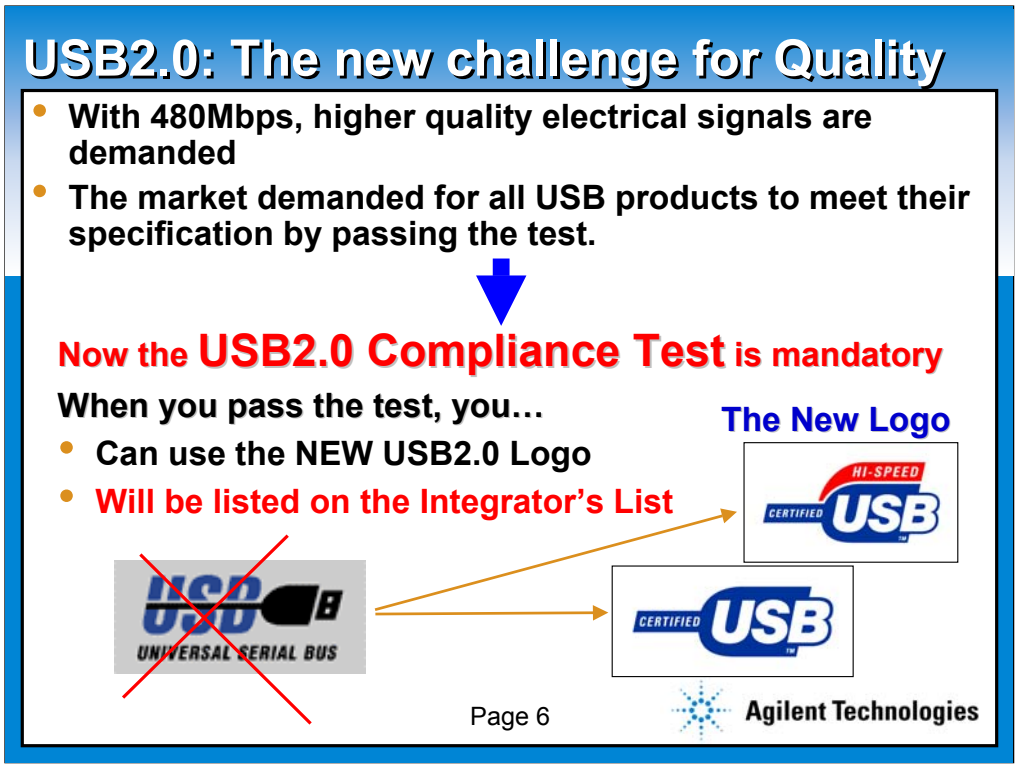
In this slide, I'll explain electrical characteristics of the USB2.0.

The signal rate for Low Speed and Full Speed will be 1.5Mbps and 12 Mbps respectively. They both have the signal level of 3.3V. The rise time values are specified on the chart, as they are a very important criteria when engineers are making the measurement.

For the hi-speed, signal rate will be increased to 480Mbps and the signal level will be 400mV. Again, it is important to know the fastest rise time allowed for hi-speed USB2.0 will be 500ps, which indicates one needs about 1GHz bandwidth to measure the signal.

Moving on to page 6.



So, with the signal rate increased to 480Mbps, the quality of the physical layer signal become very important. At the same time, the the market still demands for the stable quality product for all the USB product, even with the faster speed. In another words, the market demands all the USB products to meet all of their specifications.

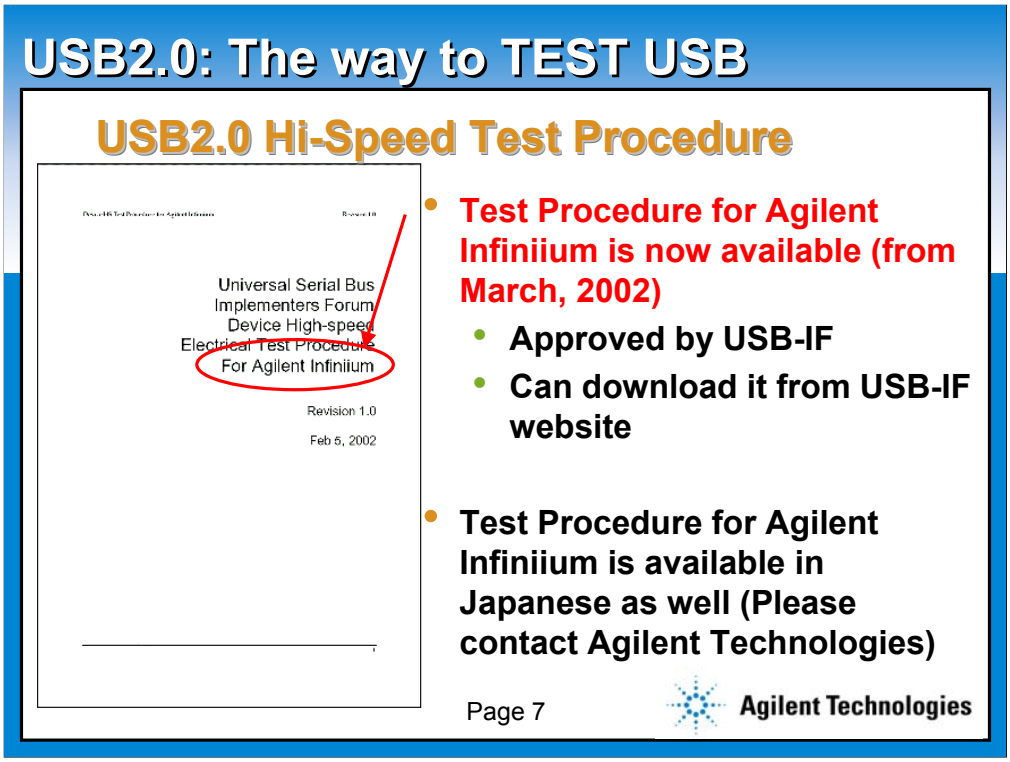
The answer from the USB-IF is the USB2.0 Compliance Test, the new challenge for the quality. Now the USB2.0 compliance test is mandatory to use the USB2.0 logo.

When you pass the compliance test, the vendor will get two benefits; the product can use the new USB logo, and the product will be listed on the integrator's list.

But most of all, passing the test itself shows the high quality of your product. Please pay a close look at the new logo. The term "Certified" is now used in the logo, which speaks for your quality.

So how exactly does the compliance test executed?

Moving on to page 7.



The answer is to execute according to the Test Procedure created and distributed by USB-IF. To prepare yourselves for the compliance test, simply download the test procedure from USB-IF's web page, and go through the test procedure.

For those who own Agilent Infiniium series oscilloscope, the test procedure for Agilent Infiniium is now available since March. Furthermore, if you are a Japanese vendor who is need for the compliance test test procedure, the Japanese version is available as well. Please contact your local Agilent representative for more information.

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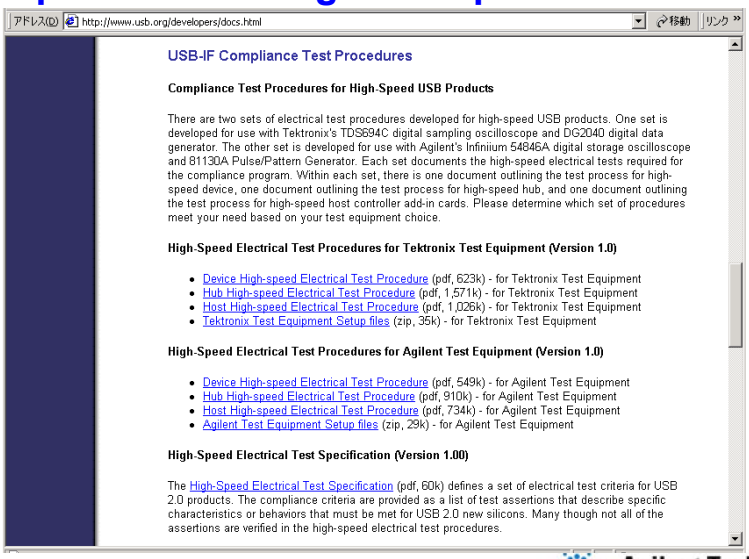
USB2.0: Info on the WEB

http://www.usb.org/developers/docs.html



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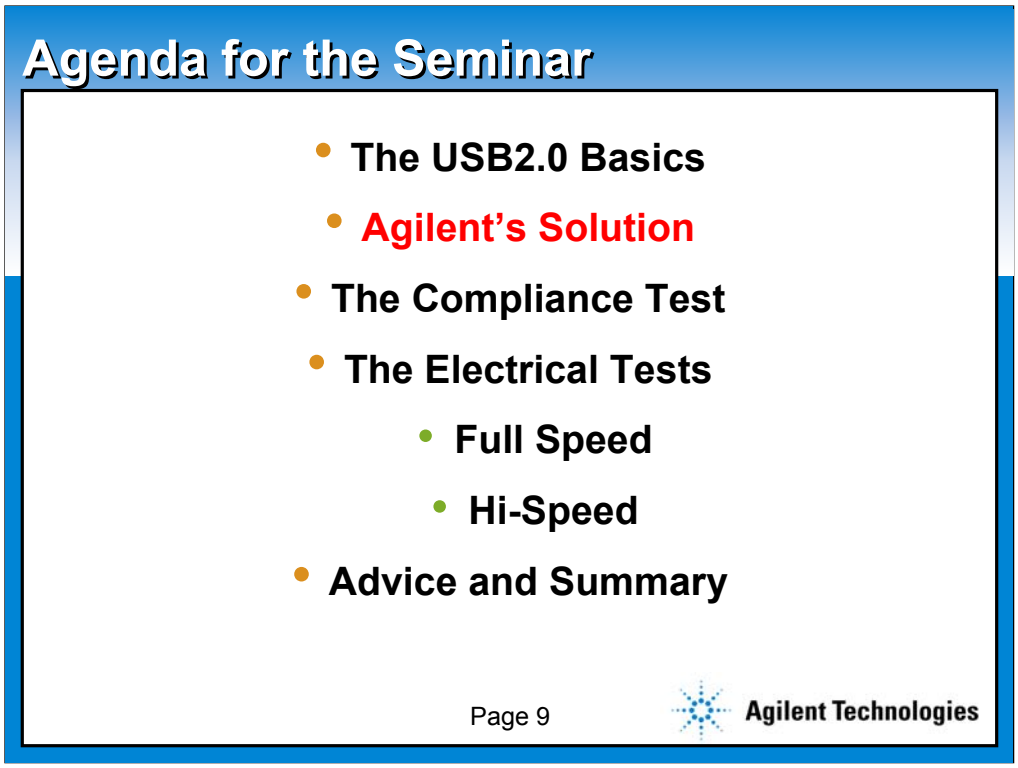
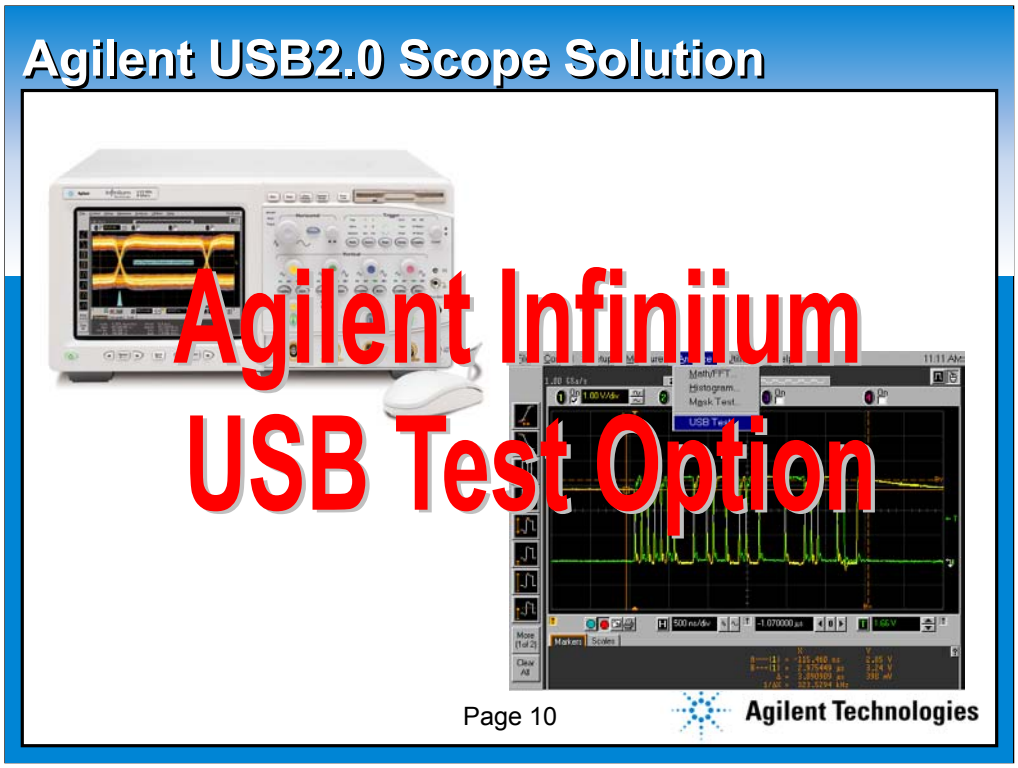
The test procedure I introduced on the previous page, and many valuable compliance test related documentations are all available from the USB-IF's home page. If you have not visited USB-IF's homepage, I recommend all to visit there ASAP.

Moving on to page 9.

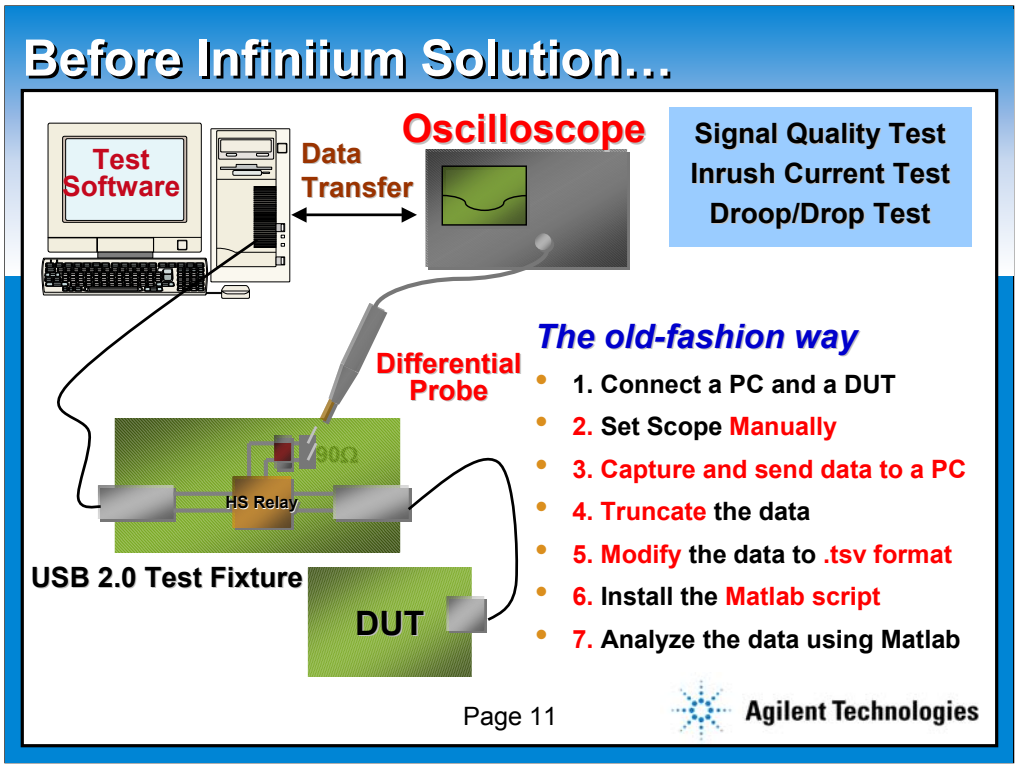


So, why exactly is Agilent providing this seminar? The reason is simple. We have the perfect solution for you all USB engineers are waiting for. Let me briefly give you the overview of our solution before I go deep dive into the details of the compliance test.

Moving on to page 10.



The name of the solution we have is called “Agilent Infiniium USB Test Option”. So, what exactly is the “Infiniium USB Test Option”?

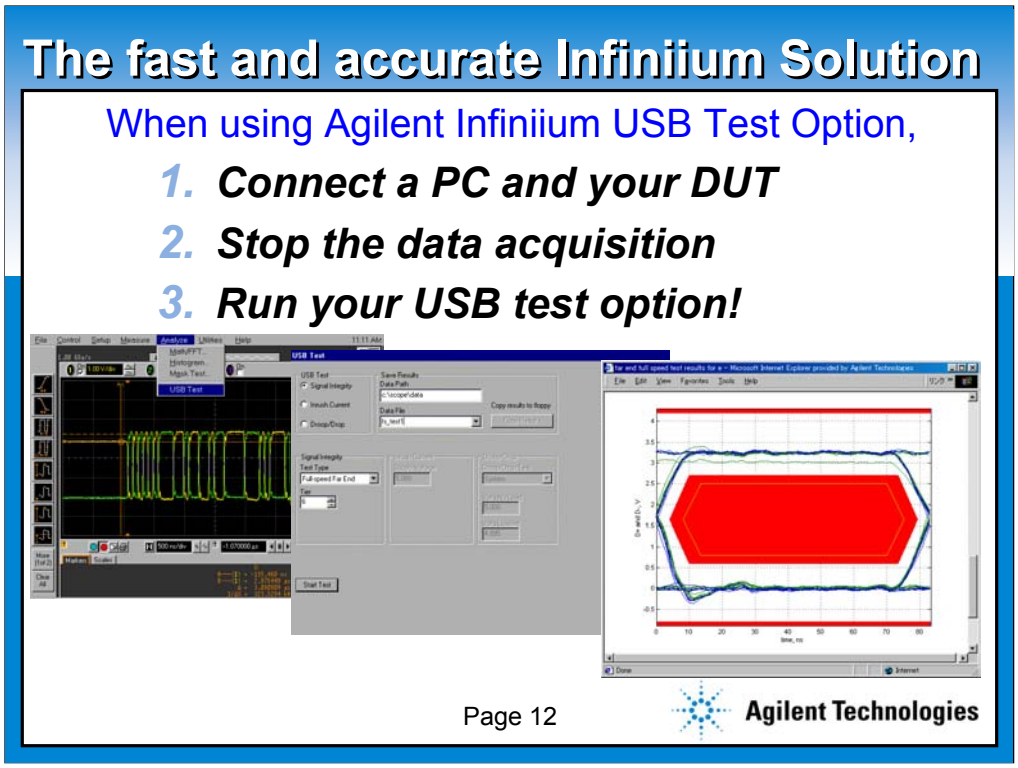


Before I explain the Agilent solution, let me provide the overview of "pre-Infiniium" way to testing USB product.

First , you must connect the PC and the DUT (Device Under Test). Then you need to manually setup your scope. Capture the data and transfer the data over to the PC. Then you need to modify the data to ".tsv format", in order for the Matlab analysis software to understand the data. Then you need to install the Matlab script, prepared by USB-IF, into Matlab software, and finally you can execute the data analysis.

Sounds pretty tough? I bet. We Agilent call all those RED FONT activities a "waste of time". Let us the Test and Measurement vendor take care this portion.

Moving on to page 12.

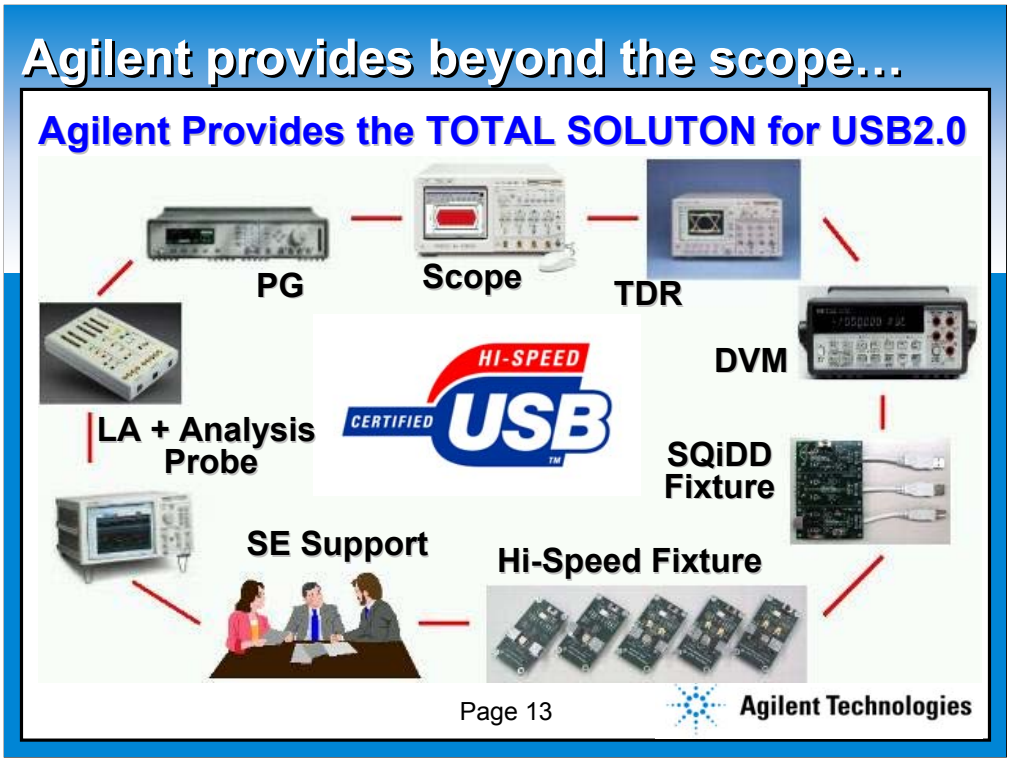


When the Agilent Infiniium USB Test Option is used, all you need to do is these three steps. Connect PC and DUT, stop data acquisition, and run your test option! It's that simple. Then, you will get the exactly the same result as you will get in the USB compliance test workshop.

With the Infiniium USB test option, you get the fast response and the accuracy you need.We achieved the accuracy by integrating USB-IF created Matlab script inside Infiniium, which is pre-installed in the USB test option. We achieved the speed by eliminating data transfer to PC and other unnecessary steps.

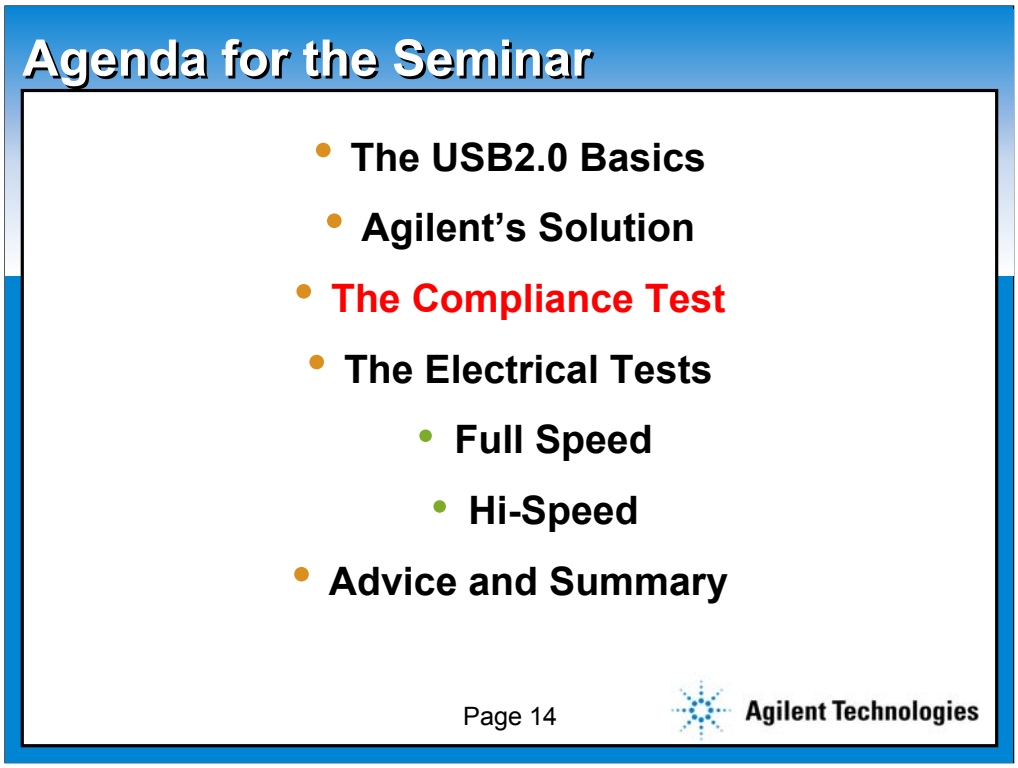
Furthermore, Agilent, being the total Test and Measurement vendor, can provide not only the scope solution, but the complete solution for your USB engineering.

Moving on to page 13.



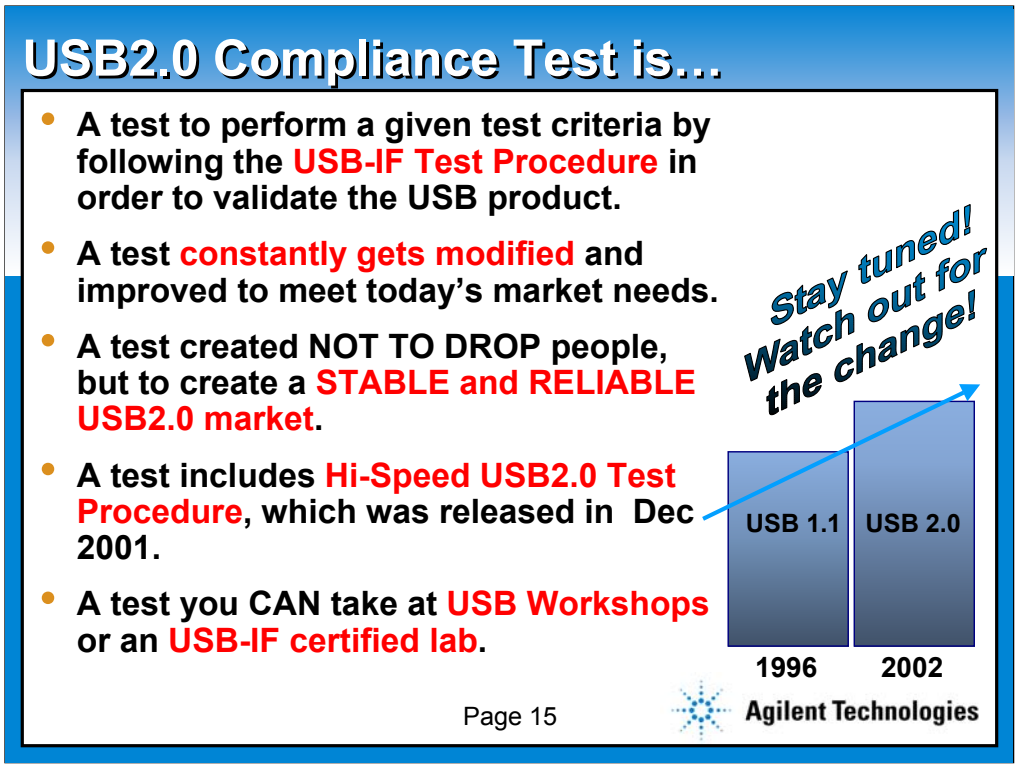
This picture shows the total solution we provide for the USB development environment. You can see Agilent provides various measuring equipments as well as the test fixtures needed for USB testing. The use of each equipment will be discussed in the following slide sets.

Moving on to page 14.



Now, let me get into the heart of the presentation, the details of the compliance test.

Moving on to page 15.



First of all, let me provide you some of the simple definitions of the compliance test.

The compliance test is :

a test to perform a given test criteria by following the USB-IF Test Procedure in order to validate the USB product.

a test constantly gets modified and improved to meet today's market needs.

a test created NOT TO DROP people, but to create a STABLE and RELIABLE USB2.0 market.

a test includes Hi-Speed USB2.0 Test Procedure, which was released in Dec 2001.

a test you CAN take at USB Workshops or an USB-IF certified lab.

The USB Compliance Workshop is a free USB member only event where you can bring your USB product to get the USB logo. This is usually held 4 times in the states and once in Asia per year. So, it is critical to schedule your product development to the USB compliance workshop, if you were considering a free test!

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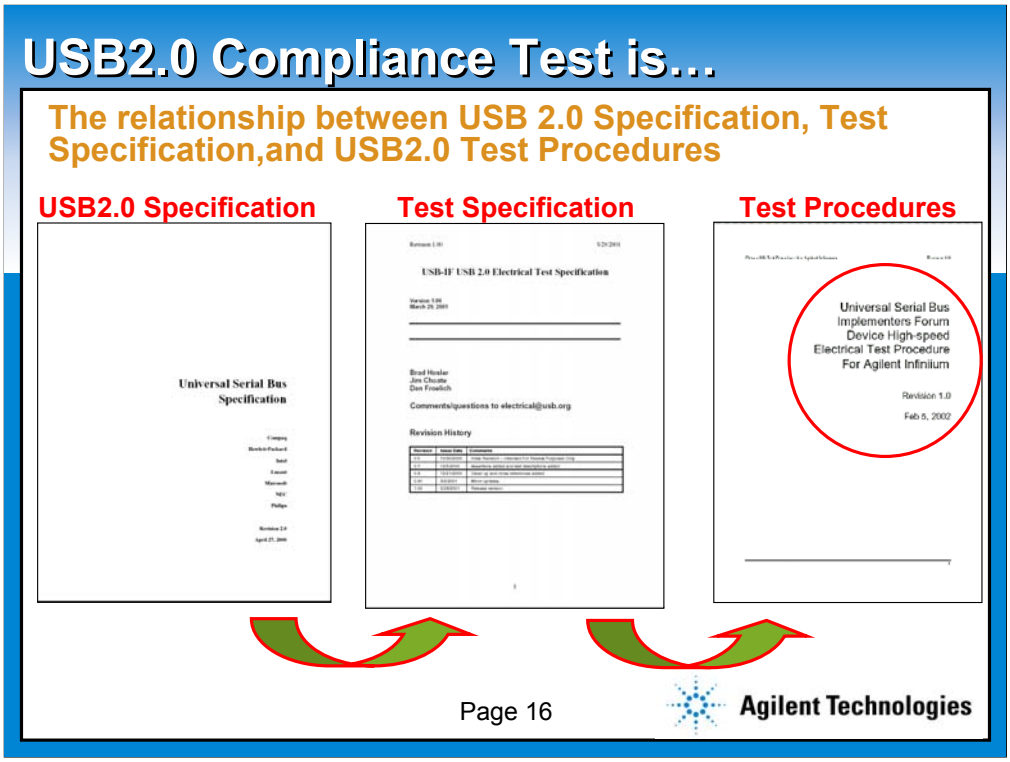
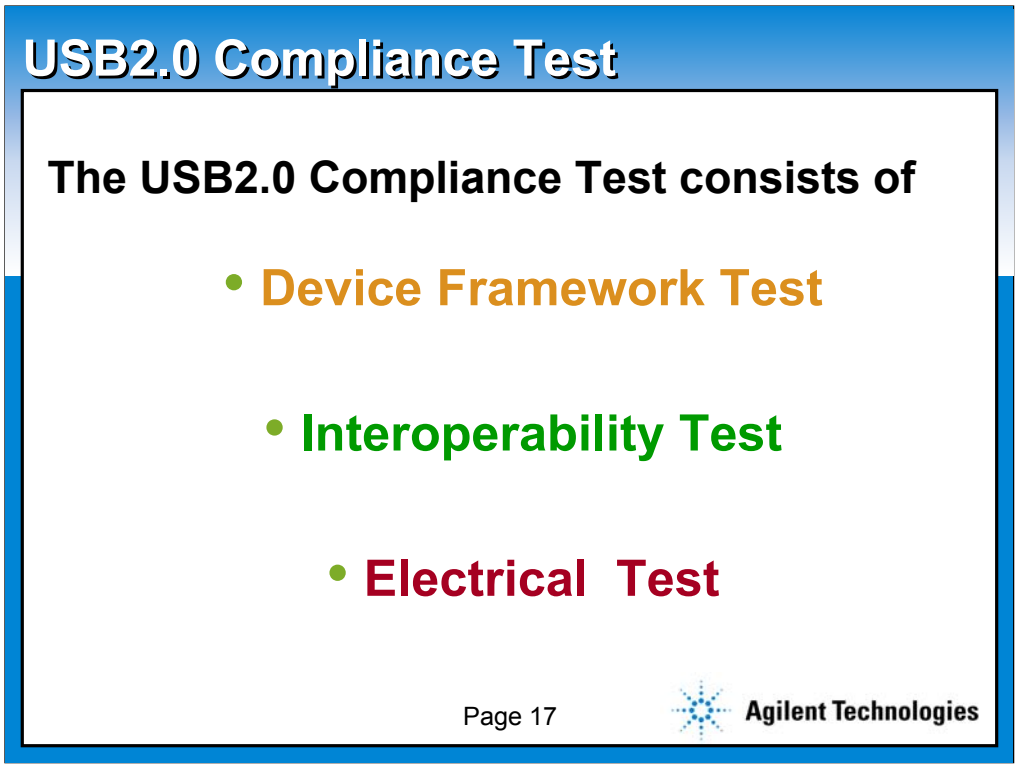


Here is the slide set to address one of the frequently asked question from our customer. There are three major types of USB documentation available from USB-IF, namely "the USB2.0 specification", "the Test Specification" and "the Test Procedure". The problem is, it is not necessary all the documentation contains the same information! So, the question we get a lot is "I find a specific test in the test specification, but test procedure does not discuss it. Which one to trust for the compliance testing?"

To make the long story simple, it is basic to design your product according to the specification. However, you do not have to execute all the test listed in the Test Specification; instead you only need to follow whatever in the latest version of Test Procedure. Just for your information, the three documents are developed in the order of "USB2.0 spec", "Test Specification" and finally "Test Procedure".

Moving on to page 17.



Now let me discuss the inside of compliance test. The compliance test is mainly consists of Device Framework Test, Interoperability Test and Electrical Test.

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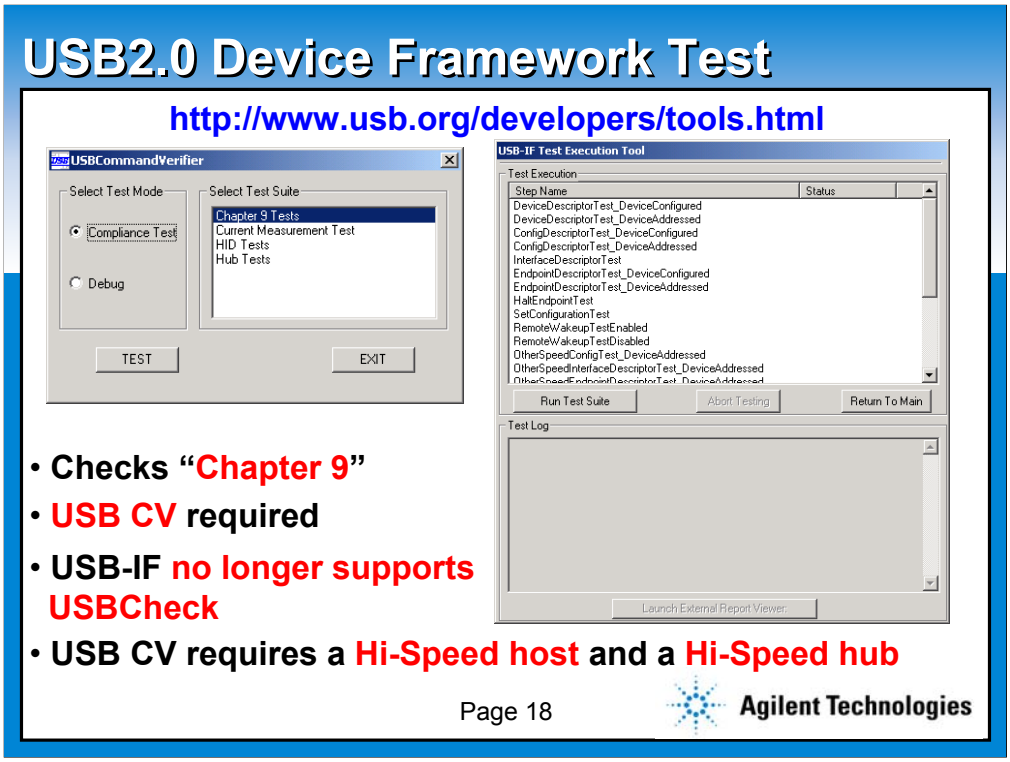

The first test is called "Device Framework Test" or usually known as a "Chapter 9 test". It is the basic of the compliance test, and is required as the pre-test session held a day before the real "compliance test workshop". In another word, you cannot even enter the test suites without passing this test!

Few cautions for this test. First of all, the old check tool called "USB Check" is no longer supported by USB-IF. Instead, a new test tool called USB CV, CV stands for Command Verifier, is the test standard now. Furthermore, in order to use the USB CV, you must have the Hi-Speed host and hub EVEN IF YOU ARE TESTING THE Full and Low SPEED products!! A lot customers forget this point , so be sure to prepare yourselves before running the test at your lab.

The USB CV can be downloaded from the given web site.

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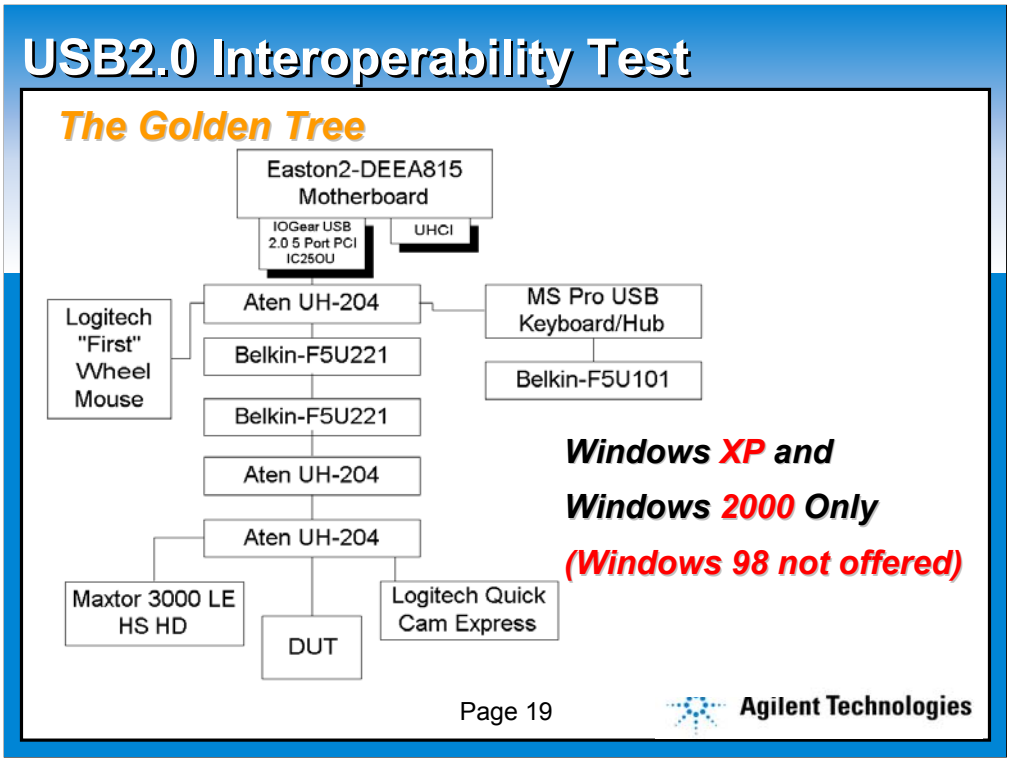

The second part of the compliance test is called “Interoperability Test”, which checks the if your USB2.0 product works with other vendors USB products as well as with various PC. At the compliance test workshop, the Interoperability Test is divided into two test sections.

The first test is done in the Interoperability Test Suite, where your product is connected to the Golden Tree shown in the slide. Your product must function properly in the given USB tree. In order for you to prepare for the Interoperability Test, we strongly suggest you to purchase the Host / Hub and Devices listed in the slide, so you can test your product with your own Golden Tree before coming to the Compliance Workshop or sending your product to the certified lab. It is also important to know that USB-IF no longer supports Windows 98. The OS on the host system must be either Windows 2000 or Windows XP.

The second test is done at various system suite rooms in the same hotel where the Compliance Workshop is held. This test will be done one on one with the system vendor where you need to successfully function your product with at least 80% of the vendors.

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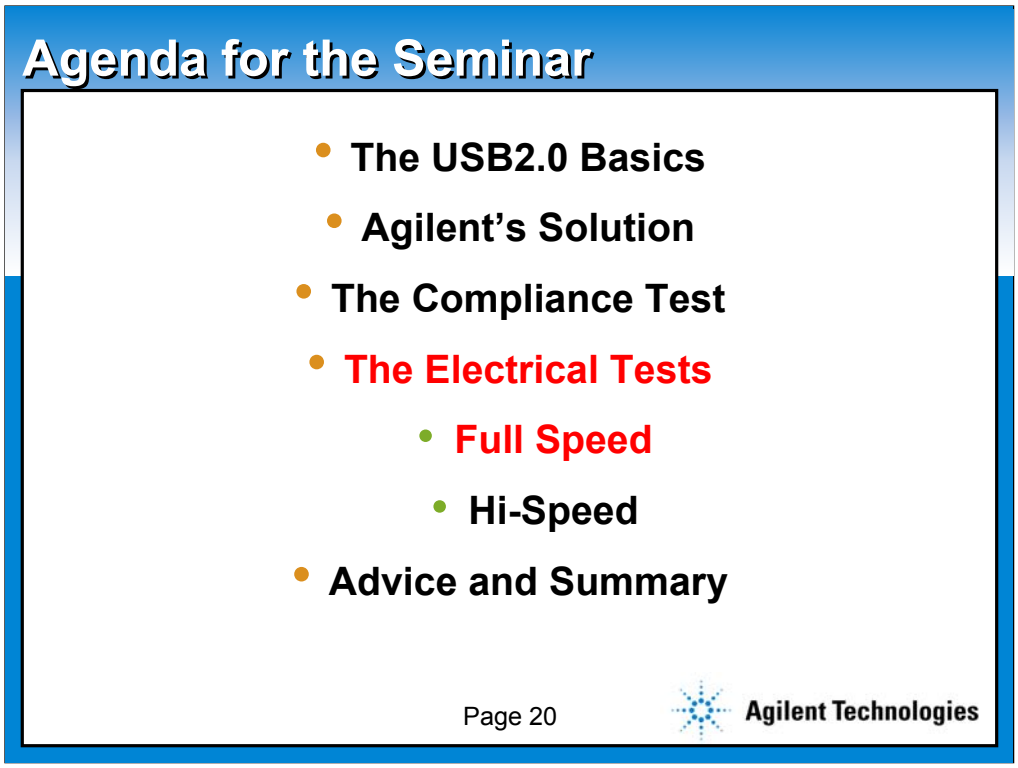
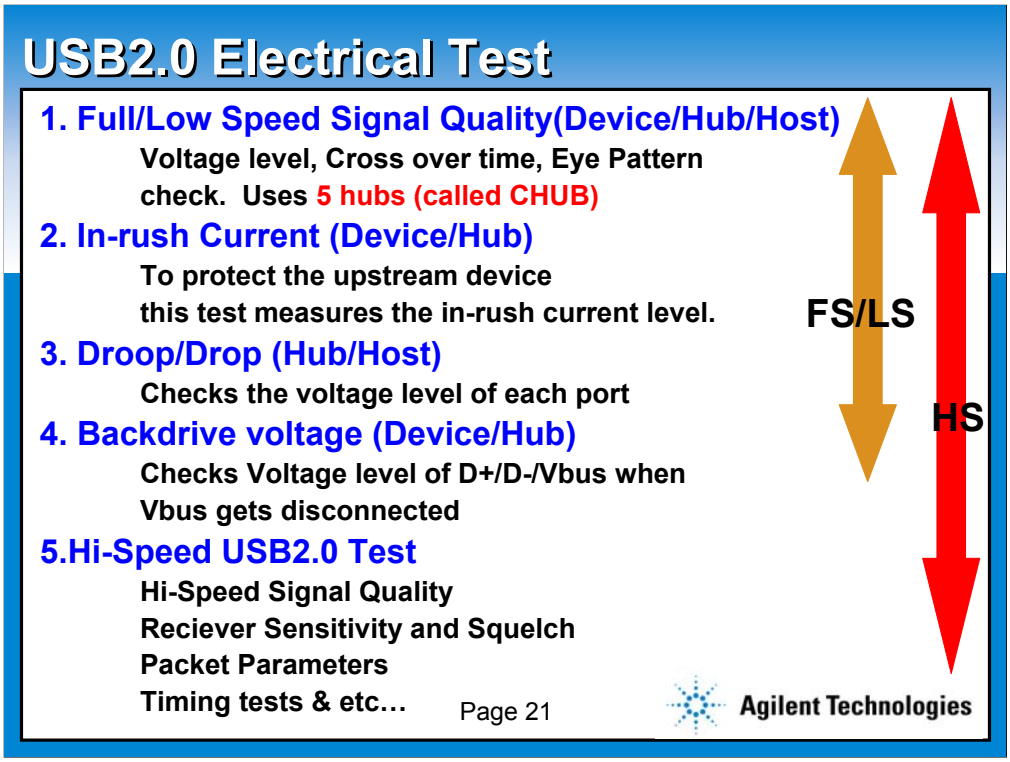


We will now discuss about the electrical tests of the USB compliance test.

Moving on to page 21.



This slide list the names of the electrical tests required for the compliance test. Please note that depending on your product, you are required to take a different tests. For example, In-rush current test only applies to Device/Hub.

For the Full and Low speed, the electrical test are consists of Signal Quality, In-rush current, Droop/Drop and Backdrive voltage test. We will discuss the details of the each test in the later section. One thing you might want to remember for Signal Quality test is that it will require a special hub called "CHUB". It is critical to know this because depending which hub you use to set up your testing environment, the test result can be slightly different.

For the Hi-Speed products, you are ADDITIONALLY required to take the hi-speed specific tests, namely hi-speed signal quality, receiver sensitivity, packet parameters, and timing tests. It is extremely important to know that your hi-speed product MUST PASS ALL THE HI-SPEED TEST AS WELL AS ALL THE FULL SPEED TESTS. A lot USB developers think that hi-speed product only needs to pass the hi-speed tests, but that is not true.

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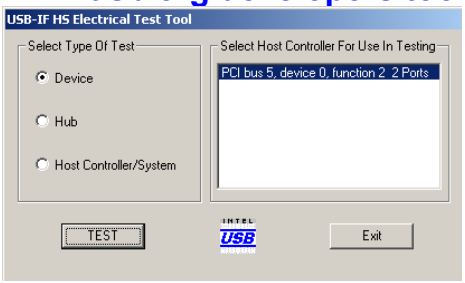
USB2.0 Electrical Test: Required Tool

HS Electrical Test Tool

http://www.usb.org/developers/tools.html



Electrical Test Bed Computer Environment:

- Pentium ® III class or equivalent processor
- 128MB or more system memory
- Motherboard with PCI Rev. 2.2 expansion slots
- Network adapter or modem adapter for supporting Internet access
- The electrical team currently uses Intel D815EEA motherboard
- Windows 2000 or XP

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In order to run USB compliance test, you must first download the tool called “HS Electrical Test Tool” from the USB-IF’s homepage.

One of the question we’ve been asked a lot is the recommended bed PC environment. The info on the slide is directly copied from the Compliance Test Test Procedure, so this should set you some standard for setting up your testing lab. Just for your information, we have successfully run the HS Electrical Test Tool on many different types of PC.

Moving on to page 23.

USB2.0: The Signal Quality Test

5 CHUB (hubs) are connected for the test.

From USB Plugfest, Jan 2002
(Full Speed Signal Quality Room)

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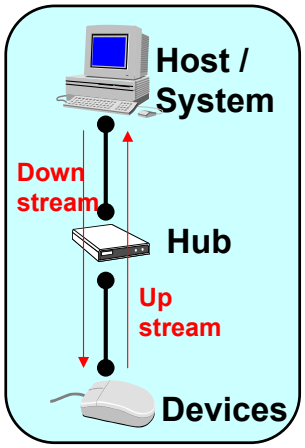
Agilent Technologies

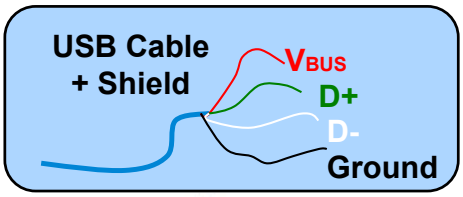
Now, we want to discuss more deep dive info about the Signal Quality Test, one of the most interesting test in the electrical test. The picture shown in the slide is from the January compliance workshop, where our Infiniium USB test option was used for the Full Speed test suite. Please notice that there are 5 CHUBs been used to create the testing environment.

Moving on to page 24.

USB2.0: The connection

- **USB Architecture**
  - Differential Signal
  - Max USB cable length of 5m
  - Up to 5 Hubs
  - Data from PC to the device is called Downstream
  - Data from device to PC is called Upstream





Agilent Technologies

This slide is here to just refresh your memory. Remember USB architecture allow up to 5 hubs connected with 5m cable. In another word, five hubs and five 5 meter cables will create the worst case test environment.

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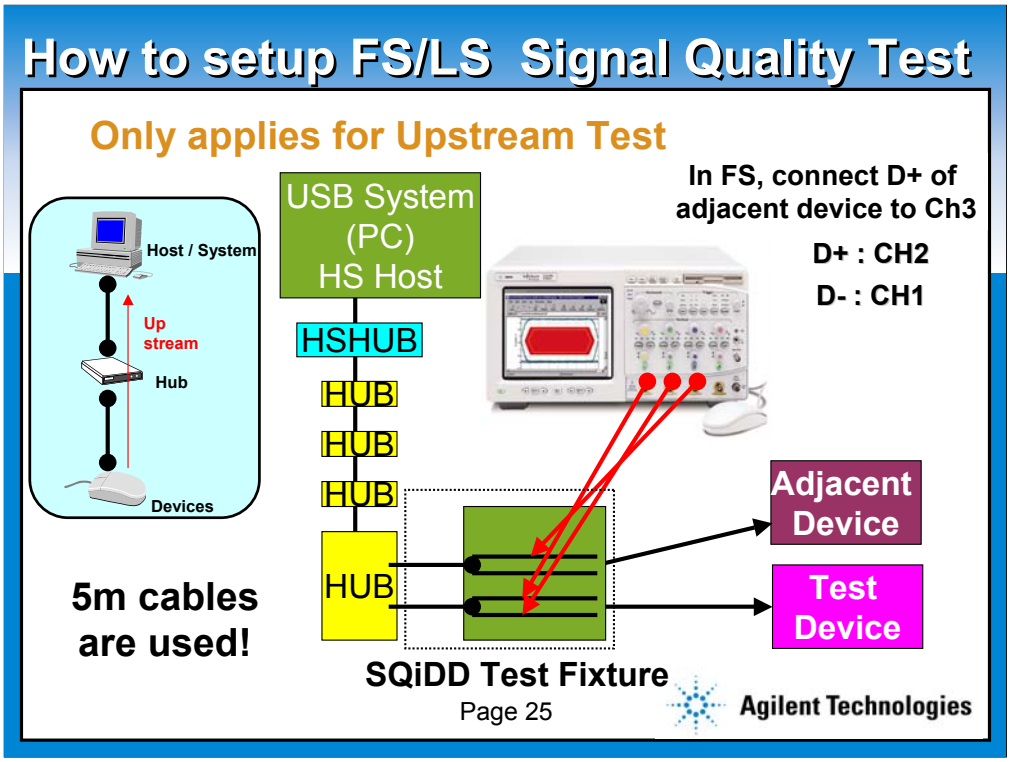

So, as you have guessed, when testing the Full and Low speed signal quality, the worst case scenario is used above. The picture illustrate how the setup will look like. In order to probe the signal correctly, a special Test Fixture called SQiDD Board is used to provide the probing point. Agilent offers E2646A SQiDD board to complete our solution.

The figure on the slide illustrates the specific setup for the upstream test, which test the Device in this example. Please note that one need to provide an adjacent device of the same speed in order to create a proper trigger condition. Although this info is specifically written in the Full and Low Speed Test Procedure, many customers have forgotten to add an adjacent device and called us for the help.

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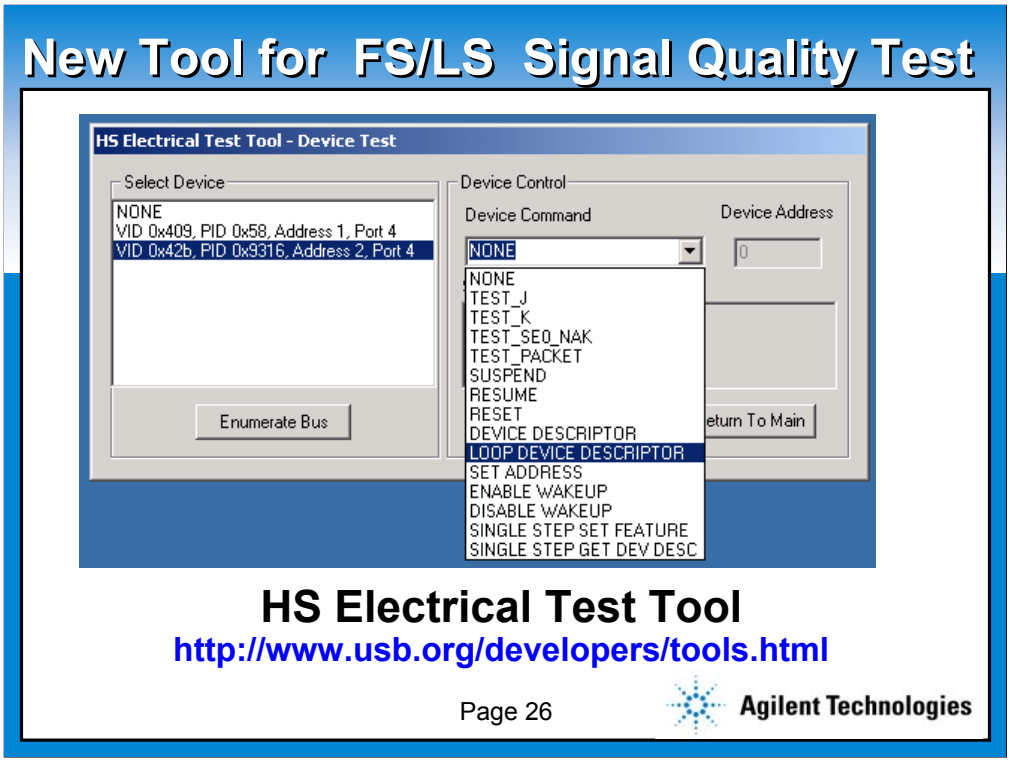

On the Bed computer where the hi-speed USB2.0 host is installed, you must install the HS Electrical Test Tool which I described before.

In the previous test procedure, the USB Check was used as the control software. Please note that from this April, the test procedure has been modified and now it is required to use the HS Electrical Test Tool for FS/LS testing as well.

For the FS/LS test, the only command you need will be LOOP DEVICE DESCRIPTOR. Just for your information, if you have used the USB Check before, you have looped the GET DESCRIPTOR command as well, so in a sense, not much has changed from the previous tool.

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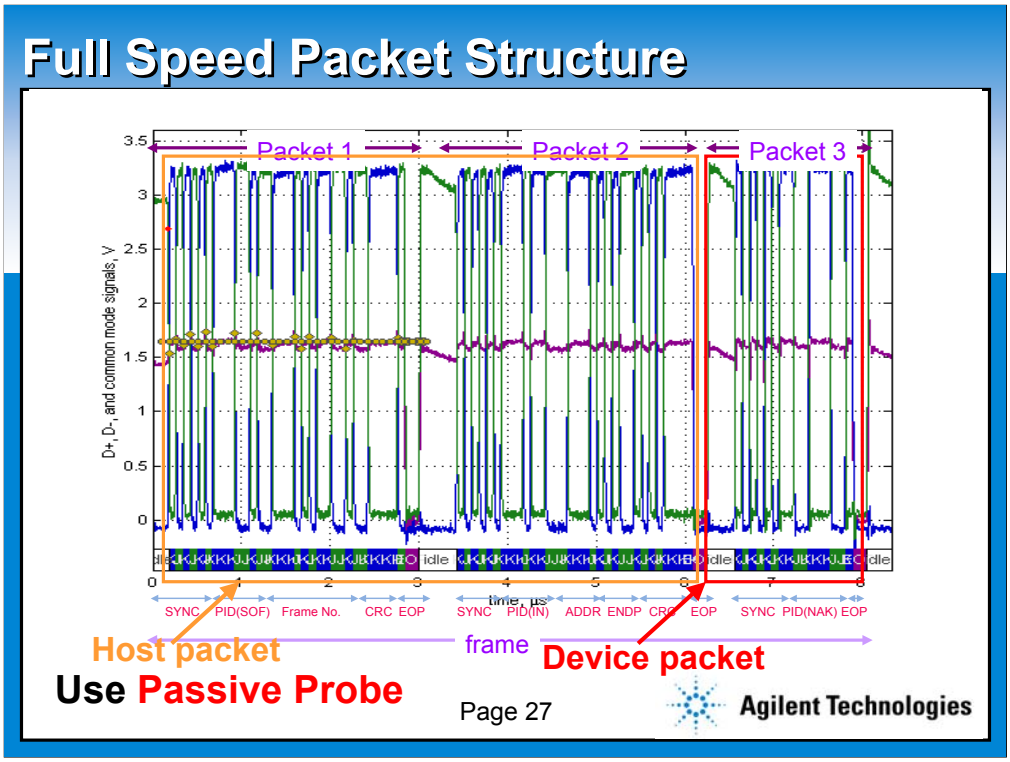

In this slide set, the picture shows an example of an USB frame. It is important to know that all the USB transaction is initiated from the Host, hence the host packet always comes before the device packet. In this example, the first two packets are from the host and the last packet is from the device.

Also, it is important to know that an adjacent USB device must be idle when the target device is talking. So if we capture the waveform for the adjacent device in Pg 25 at the same incident, you will not see any packet at the Packet 3 location.

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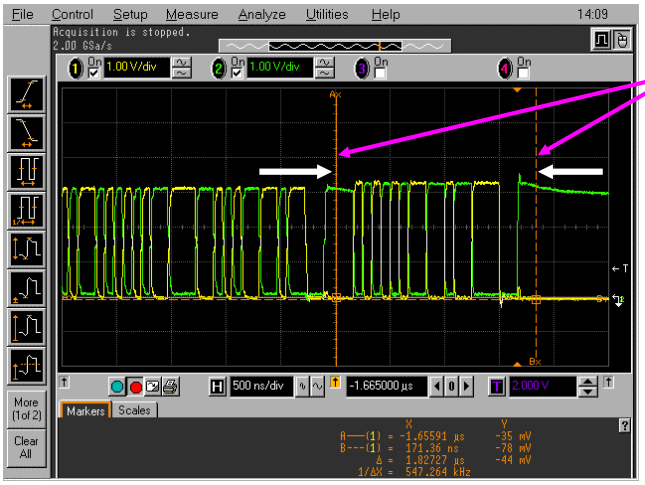
FS Signal Quality Test



Marker will be place around the device packet under test. (markers should be placed 1 bit before and after the packet)

Agilent Technologies

Here is the live picture from Infiniium oscilloscope. It will be the similar transaction from the previous slide. When you use the setup file from the Infiniium USB test option, it not only sets up the scope in the correct timebase and volts per division, but it automatically places the markers around the device packet, the packet of interest. Whatever the data between the marker will be transferred to the Matlab analysis script. One may need to adjust the marker location if needed.

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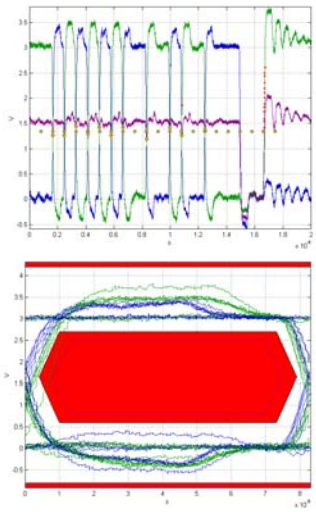
Full Speed USB2.0 Example Test Result

Far End Full Speed Signal Data and Common Mode Voltage

Overall result: pass!



•Signal eye:
*** eye failure! (14 data points violate eye) ***
*** waiver granted. ***

Waiver Granted : The result is a little over the limit, but still quality the test.

•EOP width: 170.2029ns EOP width passes

•Receivers: reliable operation on tier 6 receivers pass

•Measured signaling rate: 12.027740MHz signal rate passes

•Crossover voltage range: 1.1982V to 1.4441V, mean crossover 1.3339V
(first crossover at 1.2662V, 10 other differential crossovers checked)
*** crossover voltage failure! *** (minimum 1.3000V, maximum 2.0000V)
*** waiver granted ***

•Consecutive jitter range: -1703.52ps to 2268.87ps, RMS jitter 1183.81ps
Paired JK jitter range: -1106.65ps to 0.00ps, RMS jitter 576.53ps
Paired KJ jitter range: -584.58ps to 0.00ps, RMS jitter 409.71ps
*** jitter failure ***
(max consecutive jitter 2000.00ps, max paired jitter 1000.00ps)
*** waiver granted ***

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Agilent Technologies

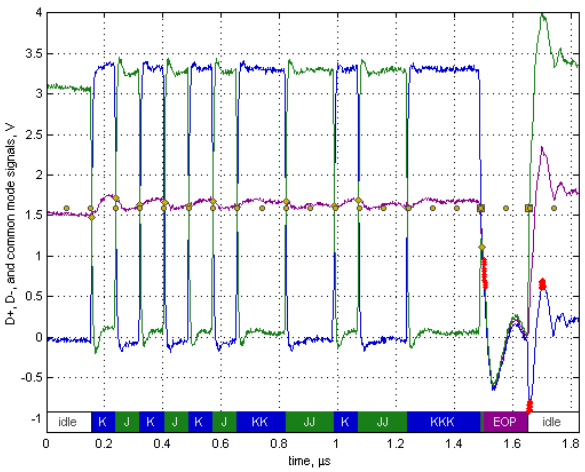
This is an example of the result of the Matlab script. It gives the automatic result of overall test result as well as each specific tests. The test criteria are "Signal Eye", "EOP (end of packet) width", "Receivers reliable operation", "Measured signaling rate", "crossover voltage" and "jitter".

One of the question we've been asked the most is about the "waiver" info shown in this example. Our customers ask "why do I pass the overall result even if I get the failure in specific items?". The answer is because of the waiver limitation. As said on slide 16, USB has three different documents. In the case of "waiver", your product not exactly matches the USB specification, but it would be good enough to pass the "compliance test test procedure document". A few things to note about the waiver is

1. **Can be changed without a notice**
2. **Some items may not have the waiver**
3. **And finally, please create your product according to the specification even though waiver is set for some items.**

Moving on to page 30.

How to read the test result - 1



Measured items

D+	green
D-	blue
common mode voltage	purple
Crossover location	yellow diamond
eye diagram reference point	yellow circle
eye violation	red dots

Agilent Technologies

This picture will show a more closer look of the data in the test result. It is very important to know what each information means. The green line indicates the D+ data. The blue line is for D-. The common mode voltage is indicated in the purple. Cross over location and eye pattern reference point are indicated in yellow diamond and yellow circle respectively. And finally, the eye violations are indicated in the red dots.

It is very important to be able to identify the eye violation points in the time domain, since eye pattern alone will not provide this valuable info.

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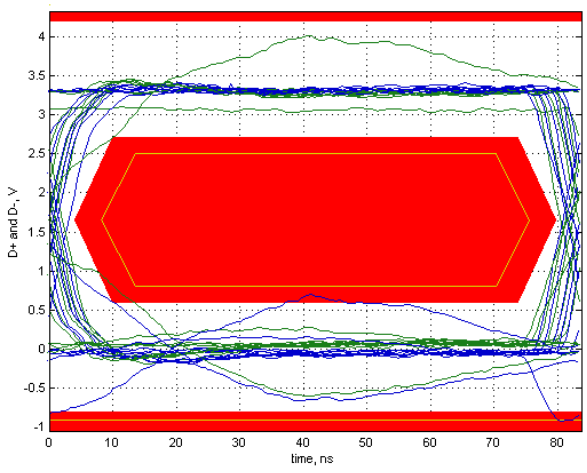
How to read the test result - 2



Measured items	
D+	green
D-	blue
common mode voltage	purple
Crossover location	yellow diamond
eye diagram reference point	yellow circle
eye violation	red dots

Agilent Technologies

This picture will show a more closer look of the eye pattern in the test result. Again, the green line indicates the D+ data. The blue line is for D-. The eye violation areas are visually viewable.

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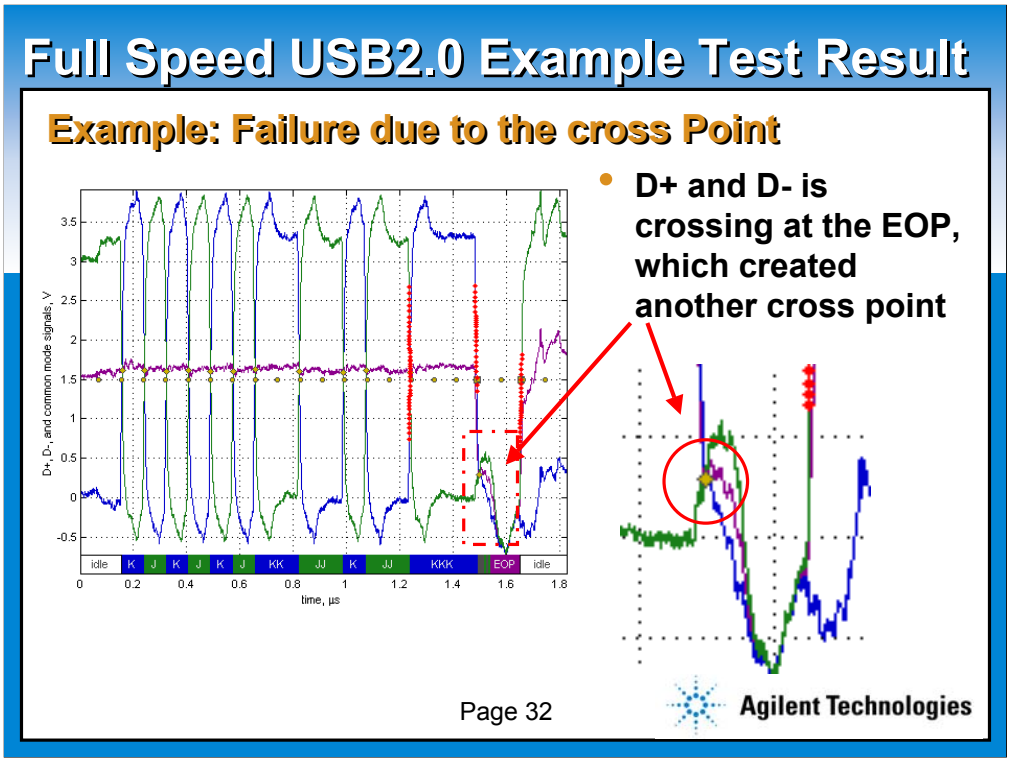

Here is an interesting example of the signal quality of EOP. This particular device failed the test due to the extra crossing point at the EOP, which should not exist. You can look at the zoomed picture where yellow circle indicates an extra crossing point.

Agilent have seen tens of these result before, and we usually find out that a wrong selection of a common mode choke or a low pass filter cause this problem. Remember, a common mode choke is a great tool to reduce the EMI, but at the same time, it will greatly influence the signal quality, especially at the EOP area. Please consult your component vendors when selecting a right items.

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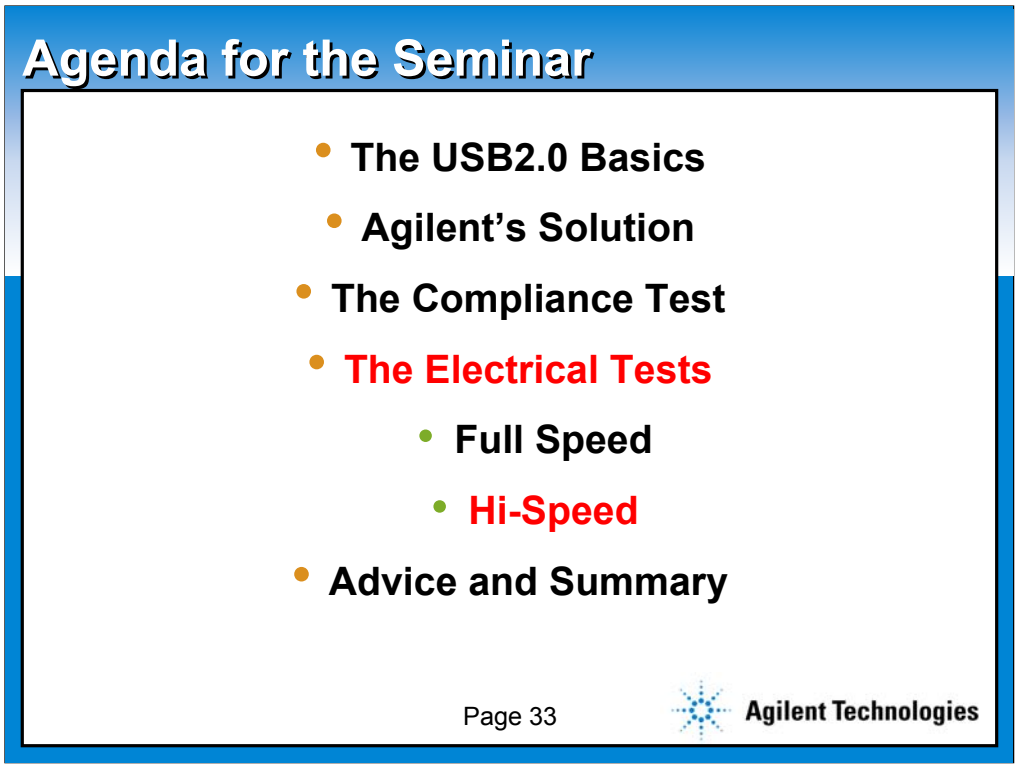

Okay, let's switch the gear to the hi-speed electrical testing, mainly on the signal quality again. The OTHER Full and Low speed electrical test will be discussed later in the section. Also, to make things simple, the test are mainly discussed for the DEVICE hi-speed testing. Hub and Host will require a little more extra test.

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First of all, for the hi-speed testing, you need a bit more than just a scope. The main compliance testing tool for hi-speed testing will be, a scope, a pulse generator, and optionally, a TDR scope.

The slide is cut and paste info from USB-IF. If shows the names of tested scopes and probes, as well as recommended requirement for the scope to be used for USB testing.

The Agilent USB solution products are listed to the right.

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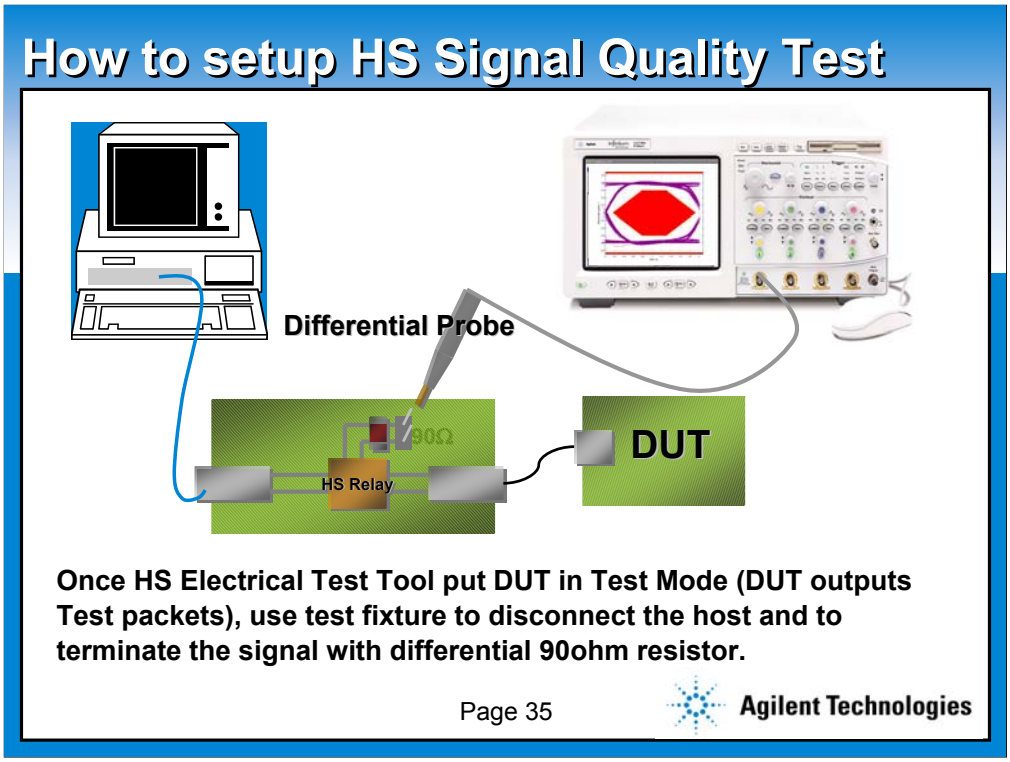

This picture illustrates the typical setup necessary for the hi-speed signal quality testing. Unlike FS/LS, you do not need to setup 5 hubs with 5m cable. However, you must prepare a hi-speed test fixture to provide the proper probing point, and a differential probe.

Just like the Full and Low speed testing, you must install the HS Electrical Tool in the bed computer to control the DUT. In this case, you will use the "Test_Packet" command of the tool, in order to put the DUT into a SELF-TALKING mode (test mode). This automatically implies that an USB2.0 Hi-Speed product MUST support a test mode in its firmware. Some of our customers did not implement the test mode in their product, so please pay a special attention.

The test fixture will provide two functions.

1. A probing point

2. 90ohm ideal termination

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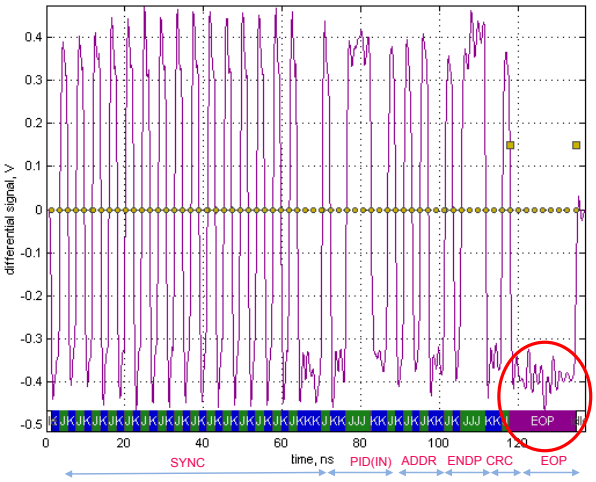
Hi-Speed Packet Structure



Signal Amplitude: 400mV

SYNC bit: 32bit (12bit min)

idle : SE0

Definition of EOP: NRZ 01111111 w/o bit stuffing

Use differential probe only

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Agilent Technologies

In the hi-speed signal, there change in the definition of EOP from the full speed. Please note that EOP is no longer a single ended zero condition (SE_O), but it is a 8 bit NRZ without a bit stuffing. SE_0 is now used for indicating the idle state. Also, please remember that the sync bit is now defined as 32 bit. These are EXTREMELY important concept for hi-speed USB2.0.

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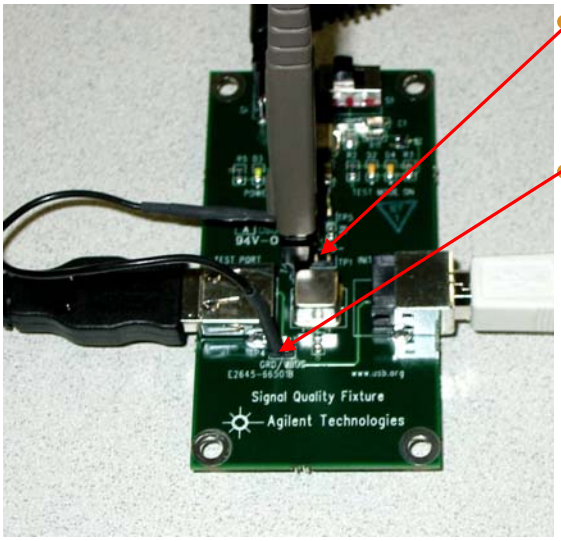
Hi-Speed Test Probing



- Look for the correct polarity (D+/D-)
- It is essential to connect to the ground when a laptop is used for the host.

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Agilent Technologies

Another question we get a lot from our customers is about the probing point of the hi-sped test fixture.

A few advice for the using the fixture is:

- Look for the correct polarity (D+/D-)

- It is essential to connect to the ground when a laptop is used for the host.

Please consult Agilent for a further question.

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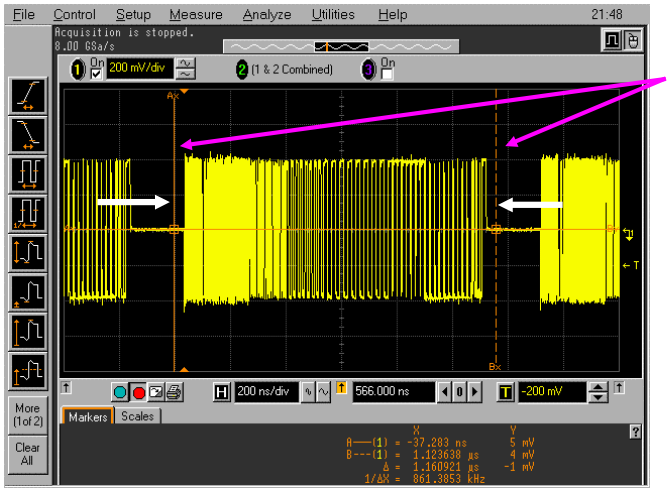
Hi-Speed Signal Quality Measurement



Area of interest (set the marker 4 bit in front and back of the packet)

Device outputting a test packet (Device is a test mode)

Agilent Technologies

Here is the live picture from Infiniium oscilloscope on hi-speed test mode packet. Just like FS/LS, it automatically places the markers around the test packet, the packet of interest. Whatever the data between the marker will be transferred to the Matlab analysis script. One may need to adjust the marker location if needed. If the signal is not stable, one might need to adjust the hold-off time as well.

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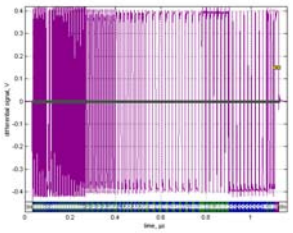
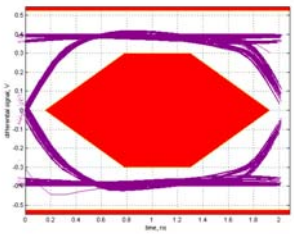
Hi-Speed USB2.0 Example Test Result





Near End High Speed Signal Quality Test
Results for test1HS

For details on test setup, methodology, and performance criteria, please consult the signal quality test description at the USB-IF Compliance Program web page.

Required Tests

- Overall result: pass!
- Signal eye:
  eye passes
- EOP width: 7.98 bits
  EOP width passes
- Receivers: reliable operation on tier 6
  receivers pass
- Measured signaling rate: 480.0641MHz
  signal rate passes

Additional Information

- Consecutive jitter range: -48.5ps to 39.7ps, RMS jitter 17.7ps
- Paired JK jitter range: -32.8ps to 34.8ps, RMS jitter 13.2ps
- Paired KJ jitter range: -41.9ps to 63.4ps, RMS jitter 19.7ps

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Agilent Technologies

Here is the example of a hi-speed test result from the Matlab script by USB-IF. The result seems very similar to Full speed test result. Measured items are

Signal Eye

EOP width

Receivers reliability

Signal Rate

Please be careful that hi-speed signal eye test will NOT have a waiver value unlike Full and Low speed.

Another difference is that the jitter measurement is NOT a part of the required test as of today. It is stated just for your information.

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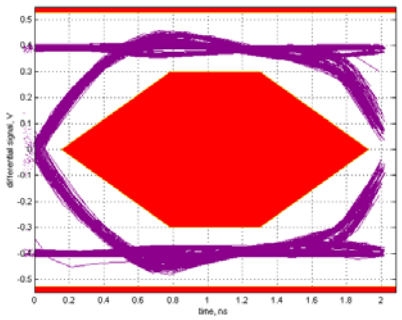
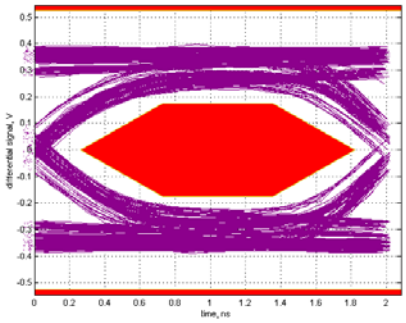
Hi-Speed USB2.0 Example Test Result

Near End vs. Far End



Upstream data of the device (B Connector upstream port) uses TP3 eye pattern (Near End)



Device with captive cable uses TP2 eye pattern (Far End) (example is shown with a 5m cable attached)

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Agilent Technologies

These two examples show difference between two eye patterns prepared for Hi-Speed testing. There are a "Near End eye pattern", where the measurement is made close to the USB silicon, and a "Far End eye pattern", where the measurement is made far from the USB silicon. "Far" end is used if and only if the product comes with the captive cable. It is essential to use the correct eye pattern depending on your product under the test. This is an area where we get a lot of questions from our customers as well.

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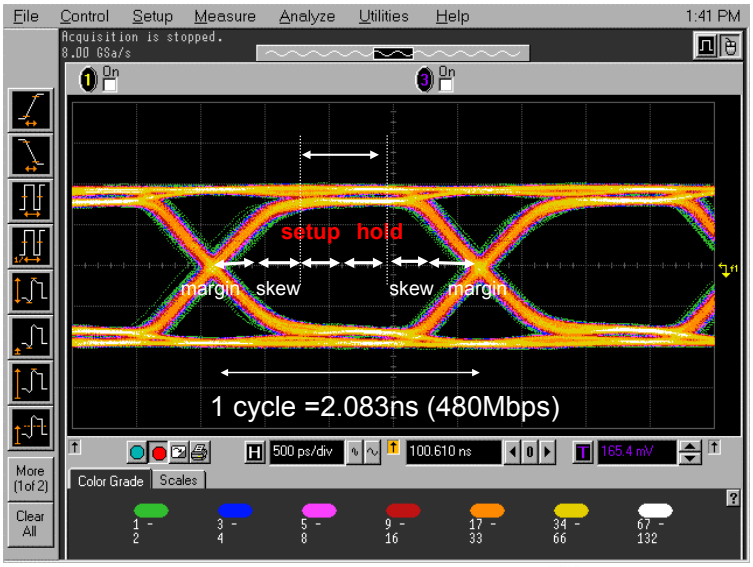
How to understand the Eye Pattern



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Agilent Technologies

This picture shows more generic way to measure the eye pattern using our Infiniium oscilloscope, without using the Matlab script.

When the engineer needs to do further investigation beyond the Matlab script, this picture should give you some good insight how you should setup your scope, and where to look for the critical parameter. You can always take the advantage of Infiniium's drag and drop measurement capability as well.

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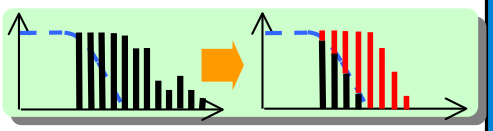
Design advice for Hi-Speed Signal Quality

- Watch out for the layout of the board
  - Keep your parallel strip line parallel!
  - Maintain the spacing!
  - Do not use the stubs!
- Correct selection of the common mode choke
  - Do not use low pass filter
  - Choose correct common mode choke
- Ground layout
  - Always pay attention to the ground layout.

$$V_{noise,\ Lm} = Lm \frac{dI}{dt}$$

$$I_{noise,\ cm} = Cm \frac{dV}{dt}$$



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Agilent Technologies

Agilent Technologies have seen hundreds of Hi-Speed signal quality testing and their results now. From our experience, we usually give the following advice when asked.

Watch out for the layout of the board

Keep your parallel strip line parallel! This is essential to avoid the cross talk.

Maintain the spacing!

Do not use the stubs!

These advices are given from the Intel at Intel Developers Forum as well.

Correct selection of the common mode choke

Do not use low pass filter. A low pass filter will work well with full and low speed to control EMI, but not with hi-speed. As you can see from the graph, a low pass filter will truncate all the necessary high frequency components.

Choose correct common mode choke. It is essential to NOT to use some common mode choke sitting at your lab. Please consult your component device vendor for the selection.

Ground layout

Always pay attention to the ground layout.

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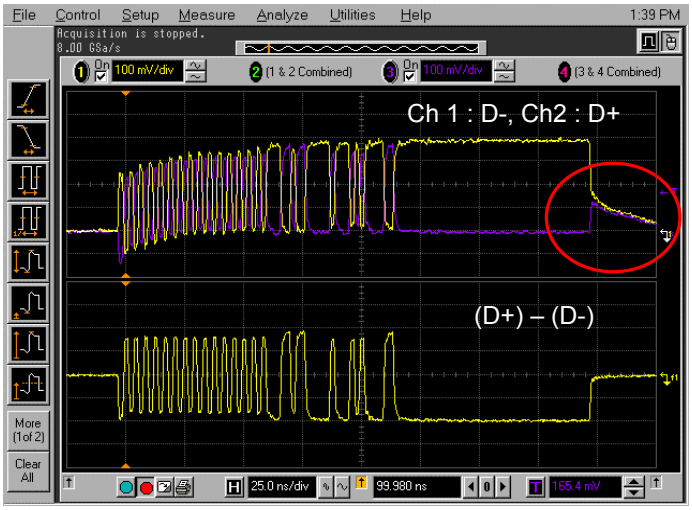
Design advice for Hi-Speed Signal Quality



A wrong selection of a common mode choke can influence the FS signal quality, without changing the HS signal quality!

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Agilent Technologies

This is a good example of what a BAD common mode choke can do. The hi-speed waveform on the top is measured with TWO single ended probe. The bottom one is the mathematical result of (D+) - (D-). As you can see, the SE_0 section of the above picture shows the distortion due to the coupling effect. So, even your selection of common mode choke will not effect the Hi-Speed signal quality, it could deeply damage the your full speed signal quality. Remember, you must pass both hi-speed and full speed tests to pass the hi-speed compliance test.

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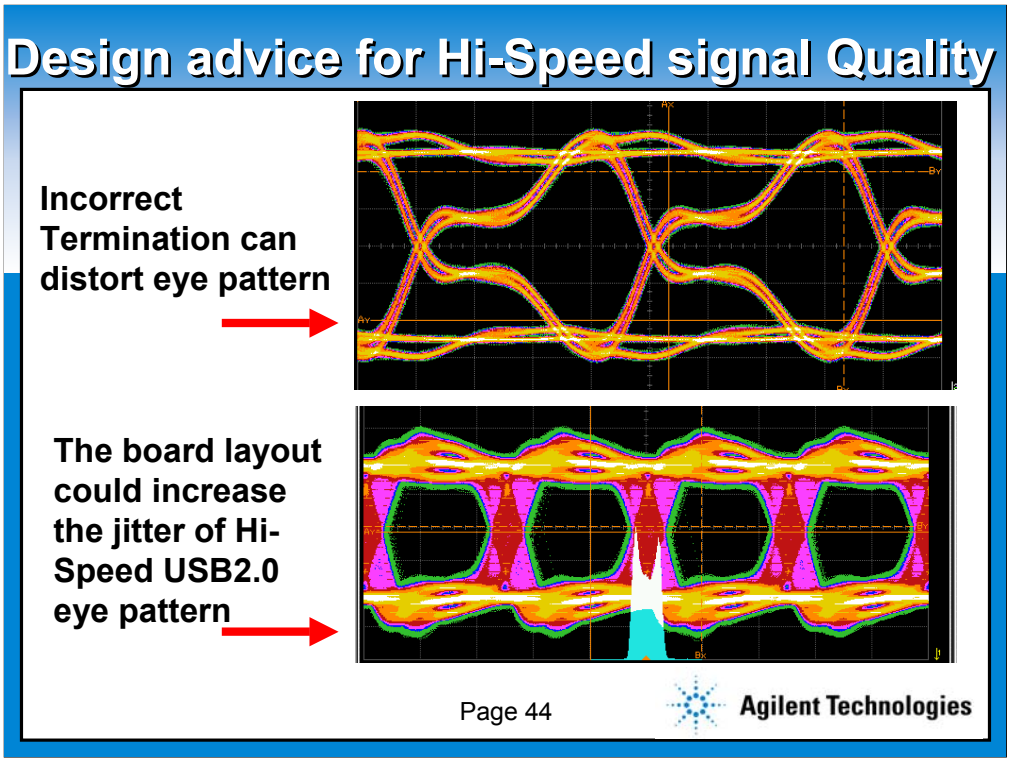

Here are some other example waveforms with incorrect design.

Incorrect Termination can distort eye pattern, shown in the top picture.

The board layout could increase the jitter of Hi-Speed USB2.0 eye pattern shown in the bottom picture.

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Other Full/Low Speed Electrical Tests

Inrush Current Test

- For Self or Bus powered Device/Hub
- To protect upstream product
- Scope data is in mA. Need to covert it to μC.
- Max value of 50.0 μC (waiver: 200 μC)

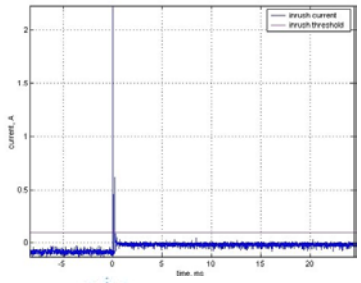
Inrush Current Test Results for inrush5

For details on test setup, methodology, and performance criteria, please consult the power consumption requirements test description at the USB-IF Compliance Program web page.

Required Tests

- Overall result: pass!
- Inrush at 5.000V: 56.63µC
  *** inrush failure! *** (at 5.000V, maximum compliant inrush is 50µC)
  *** waiver granted ***

Hot Plug (Attach) Current Draw



Agilent Technologies

So, we have looked at the various aspects of the full and low speed and hi-speed signal quality test. Now, we will briefly take a look at other electrical tests for USB2.0 compliance test.

This slide shows the example of the Inrush-current test. Inrush current test is for self and bus powered device and hub only. Since final test criteria is measured in coulomb, in the Infiniium USB test option, it will automatically calculate the coulomb value from the measured ampere value.

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Other Full/Low Speed Electrical Tests

Droop/Drop Test

- For Host/Hub
- Specification 7.2.3 "The target maximum droop in the hub V_{BUS} is 330mV"

Backdrive voltage

- For Hub/Device
- Specification 7.2.1 "No Device Shall Supply Current on VBUS at any time"
- When there is not connection with the Host, the voltage of D+, D-, VBUS must not exceed .4 Volt

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Agilent Technologies

Drop and Drop test is for host and hub only. The specification 7.2.3 says that the target maximum droop in the hub Vbus is 330mV, so this test will check this value.

The backdrive voltage test is for device and hub only. It is mainly check if the USB product is following the specification 7.2.1, which says "No Device Shall Supply Current on VBUS at any time" Droop of V_{BUS} must to be < 330mV.When there is not connection with the Host, the voltage of D+, D-, VBUS must not exceed .4 Volt.

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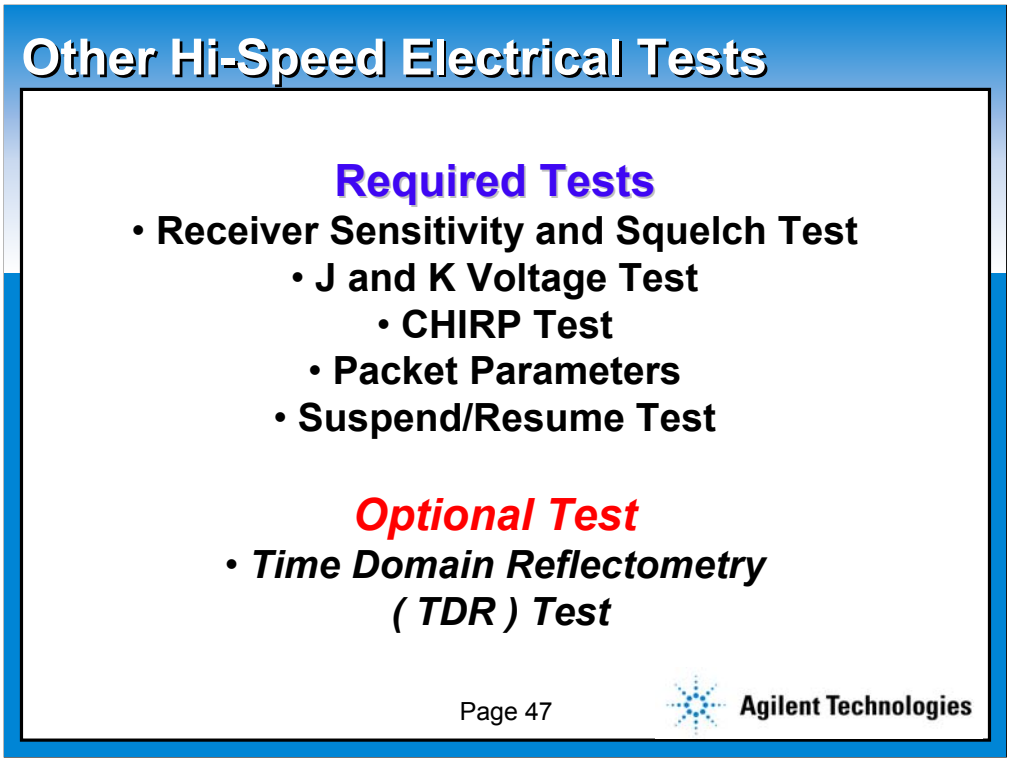

Moving onto the other hi-speed electrical tests.

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Hi-Speed USB 2.0 Packet Parameter Test

Control the device with HS Electrical Test Tool, analyze response packet from the device

EL_22 inter-packet gap should be at least 8bit but not to exceed 192bit

EL_21 SYNC should be 32bit

EL_25 EOP should be 8 bit NRZ

Agilent Technologies

In the packet parameter test, you will be measuring the Sync field, inter-pakcet gap, and EOP size. In order to execute this test, you need to use the HS Electrical Test Tool once again, to generate a special packet called single step set feature.

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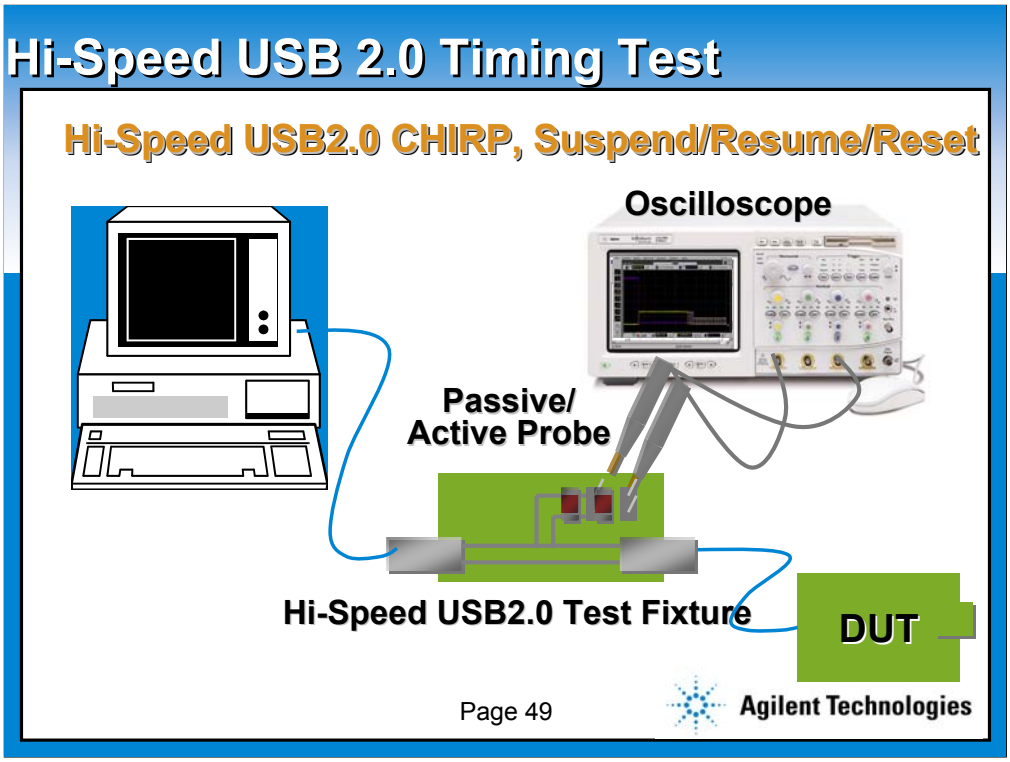

Another type of test is called a timing test, which measures the various transition timing between different state of the hi-speed USB2.0. This test is the especially important if the silicon you are using has not been certified by the USB-IF. In another words, this test mainly test the characteristics of the silicon.

The example setup is shown in the picture. You may use passive probes or active probes for this test. To save your cost, Agilent recommend to use the passive probes.

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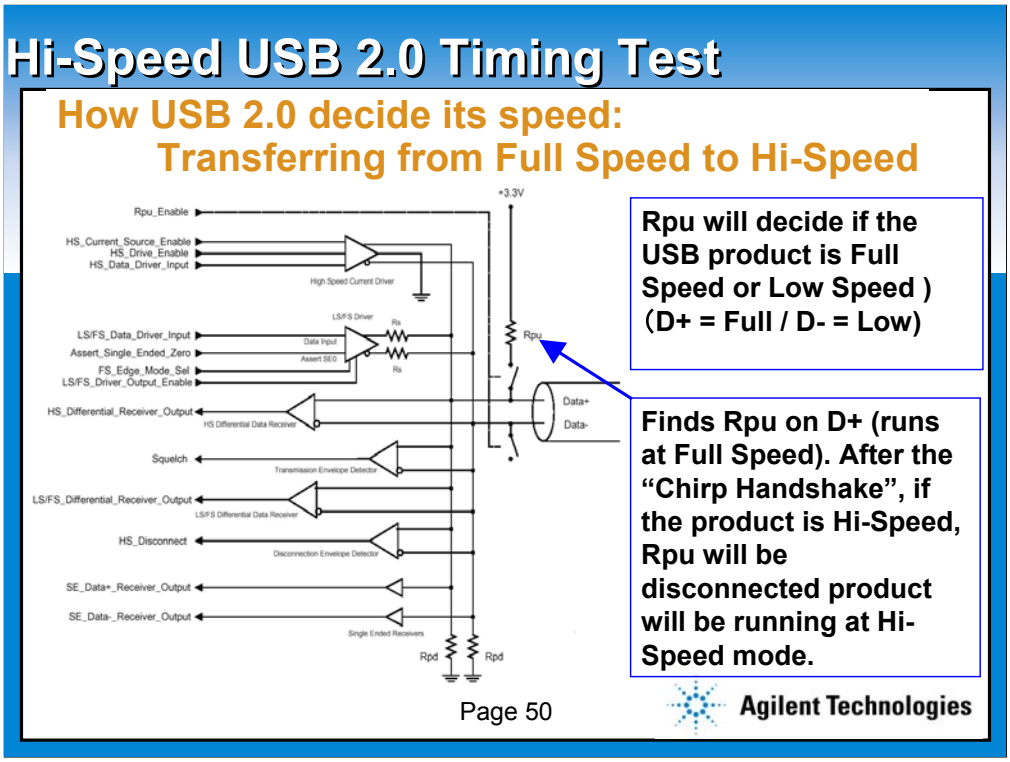

To understand the timing test, you must first understand that the hi-speed is actually a special state of the full speed USB2.0. The figure illustrates how the USB hand shake is done.

The USB product decides whether the product attached is a full speed or low speed by the location of the pull up resister. If D+ is pulled up, then it is a full speed. If D- is pulled up, then it is a low speed.

When the USB2.0 finds D+ to be pulled up, it will go through a sequence called "Chirp Handshake" to see if the product is hi-speed or not (that is why hi-speed is a special type of full speed USB2.0). If the handshake is successful, the pull up resister will be disconnected and the product will run in hi-speed mode.

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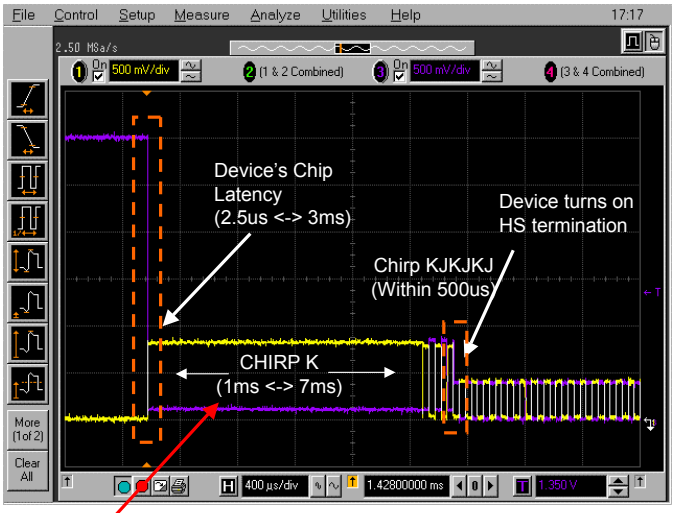
Hi-Speed USB 2.0 Chirp Test



Reset duration

CHIRP K Duration
HS termination assertion

EL_29 chirp K is at least 1ms but no more than 7ms

Agilent Technologies

So, this is the illustration showing the various specification within the chirp timing test.

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Hi-Speed USB 2.0 Suspend/Resume Test

Suspend Timing

Resume Timing

EL_38 After 3ms of idle time, device need to terminate in Full-Speed within 125us

EL_39 Device needs to get into suspend state (D+ = > 2.7V)

EL_40 Device must be able to resume. It is specified that device needs to resume in 2 bit time (FS), but all it needs is a verification of SOF.

Agilent Technologies

Other timing tests will consist of transferring time of the suspend state, the resume state and the reset. It is important to understand that when hi-speed product goes into the suspend mode, it will actually change back to a full speed mode.

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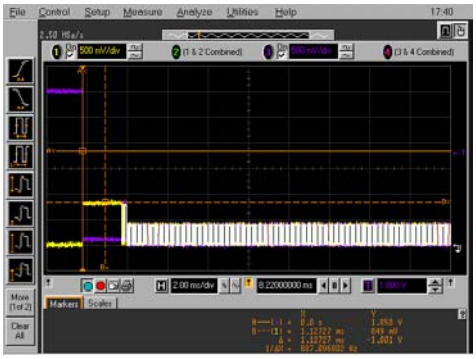
Hi-Speed USB 2.0 Reset Test

EL_27 **Devices must transmit a chirp handshake no sooner than 3.1ms and no later than 6ms when being reset from a non-suspended high-speed mode.**



EL_28 **Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.**

Agilent Technologies

This illustration shows the info on the reset testing.

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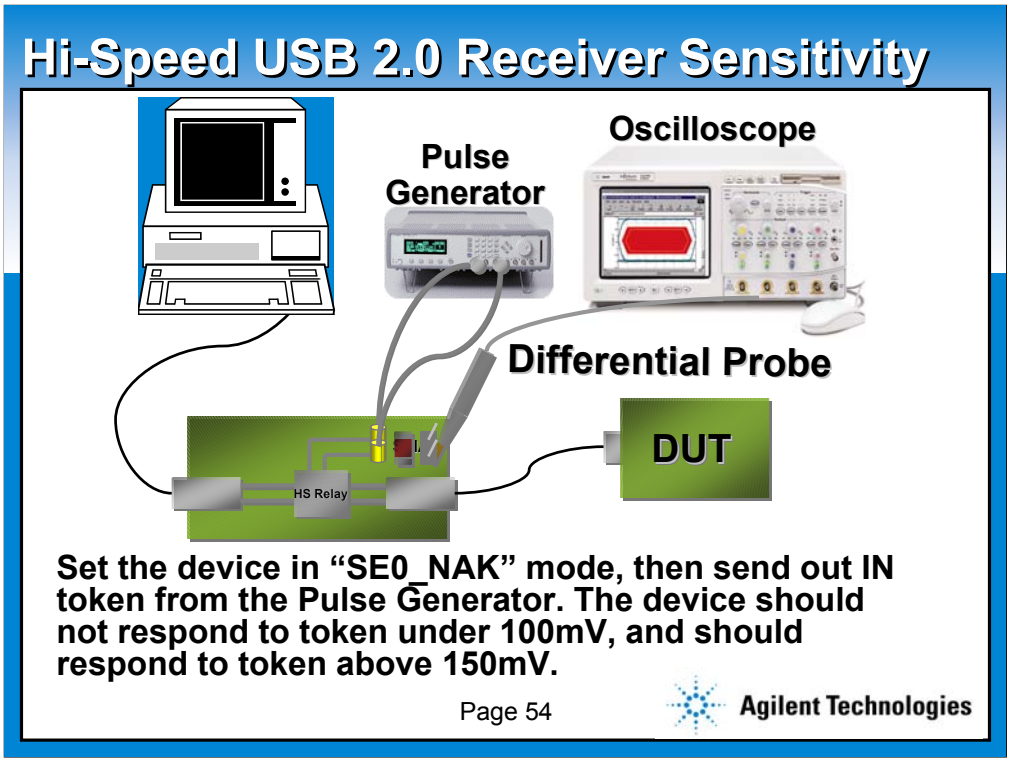

The final test to be discussed is called a “receiver sensitivity and squelch test”. The picture shows the typical setup for this test. Notice this test too requires a special test fixture, which is different from the hi-speed signal quality fixture. The main difference is that this fixture will consists of SMA cable connector for the pulse generator connection.

To do this test, you need to set the device in “SE0_NAK” mode using the HS Electrical Test Tool (TEST_SE0_NAK), then send out IN token from the Pulse Generator. Switch the HS relay on the test fixture to the pulse generator next. Finally, decrease the D+ and D- value of the Pulse Generator until you see the squelch response. The device should not respond to token under 100mV, and should respond to token above 150mV.

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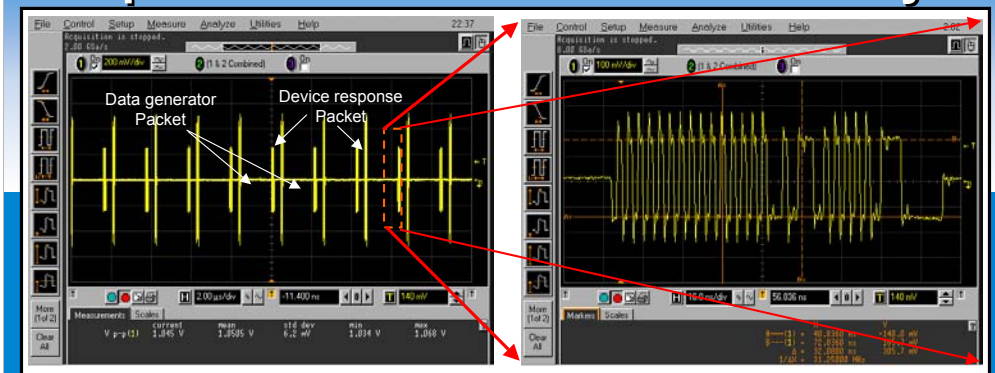
Hi-Speed USB 2.0 Receiver Sensitivity



EL_18 Hi-speed device must respond to a 12 bit SYNC packet

EL_17 A high-speed device must not indicate squelch when a receiver exceeds 150 mV differential amplitude.

Note: waiver: 150mV +/-50mV

EL_16 A hi-speed must indicates squelch when a receiver's input falls below 100 mV differential amplitude (use 32bit SYNC packet)

Note: Waiver: 100mV +/-50mV

Agilent Technologies

The picture shows the actual screen shots of the testing. Please note that you should use the voltage read out value from the "SCOPE" and not the pulse generator. The pulse generator's read out will not be the same as the scope due to:

1. We will be using attenuator in between pulse generator and the test fixture

2. Impedance difference between pulse generator and the scope input.

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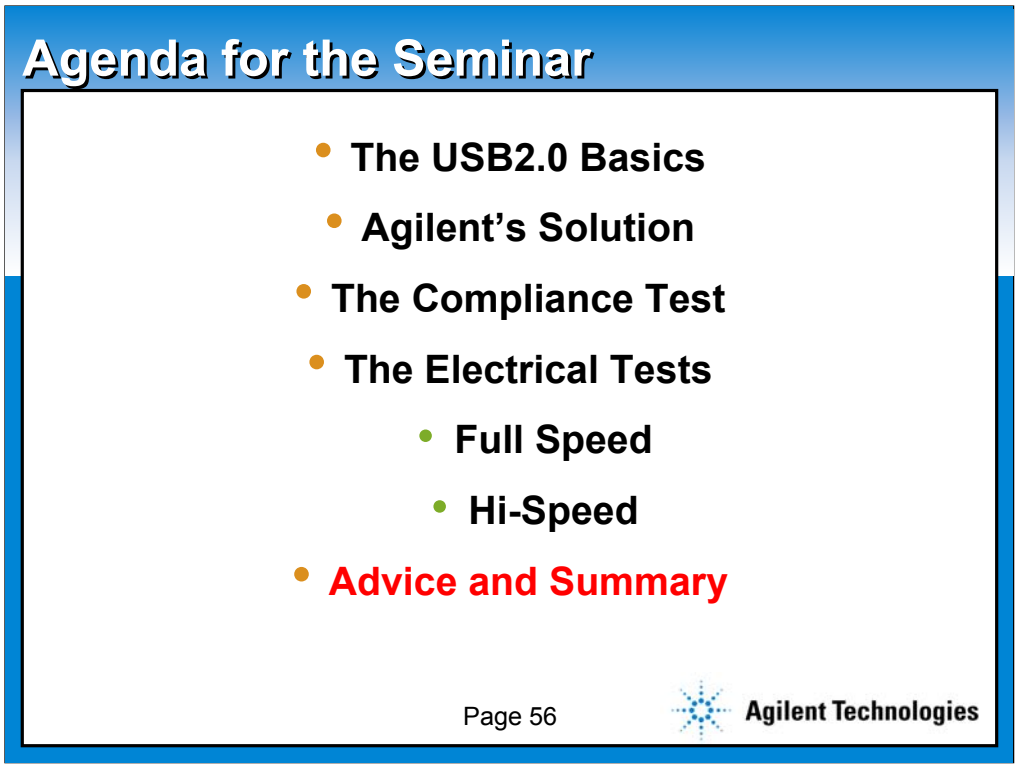

Let's move into the final section of the presentation, the advice and the summary.

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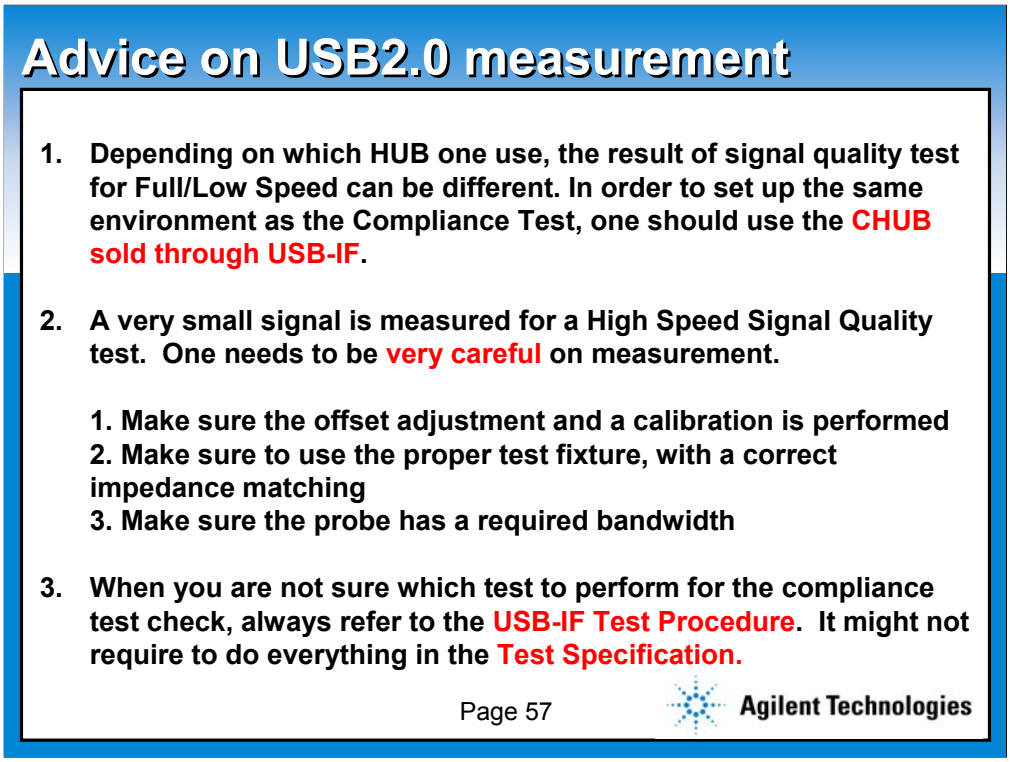

1. Depending on which HUB one use, the result of signal quality test for Full/Low Speed can be different. In order to set up the same environment as the Compliance Test, one should use the CHUB sold through USB-IF.

2. A very small signal is measured for a High Speed Signal Quality test. One needs to be very careful on measurement.

   1. Make sure the offset adjustment and a calibration is performed
   2. Make sure to use the proper test fixture, with a correct impedance matching
   3. Make sure the probe has a required bandwidth

3. When you are not sure which test to perform for the compliance test check, always refer to the USB-IF Test Procedure. It might not require to do everything in the Test Specification.

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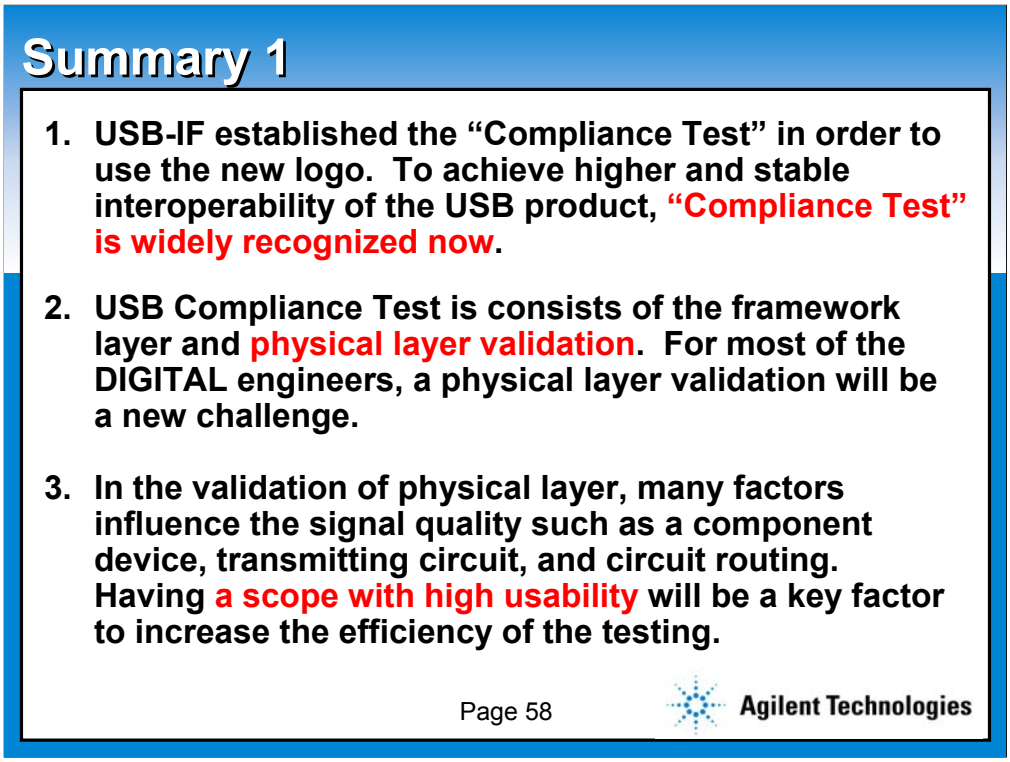

1. USB-IF established the “Compliance Test” in order to use the new logo. To achieve higher and stable interoperability of the USB product, “Compliance Test” is widely recognized now.

2. USB Compliance Test is consists of the framework layer and physical layer validation. For most of the DIGITAL engineers, a physical layer validation will be a new challenge.

3. In the validation of physical layer, many factors influence the signal quality such as a component device, transmitting circuit, and circuit routing. Having a scope with high usability will be a key factor to increase the efficiency of the testing.

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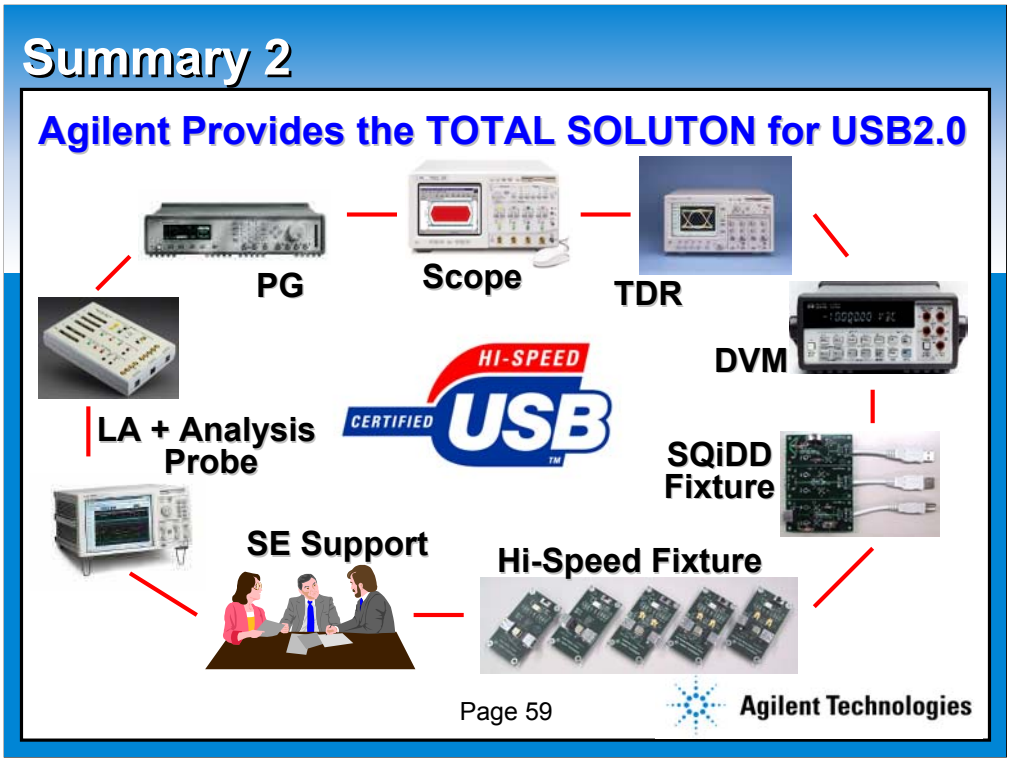

And as a total T&M company, Agilent Technologies will provide the total solution for USB2.0.

Scope:	**54846A/B**
	+ Opt B30 USB test option
TDR:	**86100A + 54754A**
Pulse Generator:	**81130A + 81132A x2**
Logic Analyzer:	**16702B**
DVM:	**34401A**
SQiDD FS/LS fixture:	**E2646A**
Hi-Speed Fixture set:	**E2649A**

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Summary 3

Agilent is a test and measurement expert in USB2.0 offering. We offer not only test instrumentation, but also consulting and training to help you gain confidence in your USB 2.0 pre-compliance test.

For more information, contact Thyda Tsai, (503) 579-6898

- **Pre-compliance test services to help in early phases of validation**
- **Additional on-site consulting to help get to root cause of failures**
- **Training on how to do pre-compliance tests using Agilent test equipment**

Agilent Technologies

Furthermore, our special SE team will be more than happy to assist you for your USB2.0 developing. Please contact Thyda Tsai at (503) 579-6898.

Thank you for your listing and your attendance!